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TIMING PULSE GENERATION FOR A SYNCHRONOUS LOGIC SYSTEM

by

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SUMMARY

A description is given of three pulse generators which produce related waveforms used in the control of a directly coupled logic system. The directly coupled transistor logic (DCTL) technique is first expounded in so far as it is relevant to the material in the text.

Each generator is considered first in general terms complete with the associated logic diagrams, and then a detailed description is given of the practical interpretation illustrated with schematic diagrams and waveforms.

CONTENTS

ILLUSTRATIONS

1 INTRODUCTION

The timing of operations in any synchronous logic system presupposes the availability of suitable control waveforms. The timing pulse system to be described was developed for a serial mode digital computer, although its application is not confined to this and was adapted to the requirements of the directly coupled elements of which the computer is formulated.

In the timing organization of a serially operated computer, it is common practice to divide the time allotted for a computation step into equal periods to correspond to the number of arithmetic operations to be performed in that step. The resulting periods, called word periods, are sub-divided according to the numerical length of the numbers to be processed at each arithmetic operation, each sub-division being named a digit period. To enable logical and timing restandardization operations to be carried out within a digit period, the latter is further sub-divided into a convenient number of phases.

Since the serial type computer is essentially synchronous, it is necessary to define each and every word period described above by pulses of identical duration which occur at the appropriate rates. The required pulse trains for the word, digit and fractional-digit periods are given the designations A, P and p respectively. Thus the word periods are labelled A1, A2.....An, the digit periods P1, P2.....Pn etc.

A brief specification for these waveforms is set out below:

A Waveforms

Repetition rate	10 Kc/sec
Pulse duration	25 microseconds
No. of waveforms per computation step	4

P Waveforms

Repetition rate	40 Kc/sec
Pulse duration	1 microsecond
No. of waveforms per word period	25

p Waveforms

Repetition rate	1 Mc/sec
Pulse duration	0.25 microseconds
No. of waveforms per digit period	4

A diagram illustrating the relationship between these waveforms is given in Fig.1.

It is the purpose of this Note to describe the means by which these waveforms are generated and tailored to the needs of the directly coupled transistor logic (DCTL) technique.

2 THE DIRECTLY COUPLED TECHNIQUE

2.1 Choice of transistor

In order to expose the requirements of pulse generators which control a system employing the DCTL technique[1,2,3,4], the latter will be expounded to the extent necessary. In any event, small parts of the generators themselves employ the technique. The transistor type which was designed specifically to realise reliable direct coupling of transistor amplifier stages is the surface barrier or micro-alloy type. The particular unit which is most readily available is the SB 240 manufactured by Semiconductors Ltd. A summary of its characteristics is set out below.

Maximum ratings

Collector voltage	-6V
Collector current	15 mA
Base current	5 mA
Total dissipation at 25°C	30 mW

Switching parameters

	Minimum	Typical	Maximum
Collector saturation voltage (Ic = 3 mA Ib = 0.3 mA)		60	100 millivolts
Leakage current (Vce = 4.5V Vbe = -100 mV)		70	150 microamps
Current gain βo (Vce = -0.5V Ic = 3 mA)	15		
Cut off frequency f_1	25	50	Mc/sec
Hole storage factor		86	120 nanosecs

Included also is a diagram depicting the spread of the input characteristic (Fig.2a) and another showing a typical output characteristic (Fig.2b). The information given shows that this transistor is suitable for the direct coupling of common emitter stages as illustrated in Fig.3. It can be seen that it is capable of saturating to a level below 100 millivolts and that a reasonably small collector current flows when the transistor is supplied with a base-emitter voltage of this value. It should be noted however that coupling the collector junction of one transistor directly to the base-emitter junction of the next, modifies the first transistor's output characteristic. The effect on a typical characteristic is shown in Fig.4 and due consideration should be given to it in design.

A typical rise or fall time over a collector excursion of 0.5V and when operating under saturating conditions, is 15 nanosecs. An excursion of this value was chosen because this is a typical value encountered in practice. It is limited by the constant voltage form of the succeeding transistors input characteristic. This means that the transistor must be capable of an adequate

current gain at low voltage levels and at high frequencies. The poor performance of most transistor types under these conditions is an inherent weakness, but the summary of parameters above shows that this defect is mitigated by the use of the surface barrier transistor.

The turn-on delay of a transistor is due to the finite transit time of current carriers through the base material. Since the surface barrier transistor features an extremely thin base region, the delay time is very small, typically 5 nanosecs. The turn-off delay time however is mainly due to the phenomenon of hole storage (p.n.p. transistors). This storage delay time is predictable[5], a hole storage factor being used to compare transistors working under the same operating conditions. It varies with the degree of saturation and from transistor to transistor, a 3 : 1 spread being typical. This effect is undesirable in a synchronous logic system, because it causes pulse elongation and displacement in addition to overlap between adjacent pulses. These defects can be overcome by use of the p pulses for timing restandardization, provided that the p pulses themselves are relatively free from these same defects. The difference between the maximum and minimum hole storage times likely to be encountered sets the limit to the switching speed, since if it is comparable with the shortest timing pulse, accurate timing reconstitution becomes difficult. For the SB 240 the manufacturers claim a maximum switching speed of 5 Mc/s.

It can be seen that within the limits discussed above, the SB 240 is eminently suited for use in a system of DCTL.

2.2 The directly coupled transistor 'or' gate

Surface barrier transistors may be connected in parallel to a common load resistor to form an 'or' gate as shown in Fig.5a. The function of such a gate is to combine signals originating on different paths and at the same time to provide isolation between these paths. The operation of this element is as follows:

If all the parallel connected transistors are cut off, then ignoring leakage currents, the potential at the common node will be that developed across the base-emitter junction of the succeeding transistor, typically -0.5V. On the other hand, if one or more is caused to conduct by developing -0.5V between base and emitter, the output potential will rise to the saturation level, typically 60 mV. It is seen that signal inversion takes place and an output inverter amplifier is needed to restore the signals to their original polarity. Let the saturation and the output (-0.5V) levels be denoted by 0 and 1 respectively. Table 1 shows the outputs C which will be obtained for the four possible combinations of two inputs A and B.

TABLE 1

A	B	C
0	0	0
1	0	1
0	1	1
1	1	1

Transistors are well suited for this function because of the high ratio of non-conducting to conducting output resistance. The number of transistors which may be placed in parallel is limited by leakage current considerations[3], a typical maximum being four for a maximum working temperature of 35°C.

2.3 The directly coupled transistor 'and' gate

Surface barrier transistors may be connected in series to a common load resistor to form an 'and' gate as shown in Fig.5b. The function of this gate is to provide an output only for a coincidence of all inputs.

This element operates in the following way:

If neither transistor or just one is supplied with a -0.5V input, then ignoring leakage current, the signal current will be zero since one transistor remains cut off. Under these conditions, the output potential will be the -0.5V or so developed across the succeeding transistors input terminals. If both transistors are provided with inputs however, the series chain becomes effectively a low resistance and the output potential rises to the sum of the two saturation voltages. As in the case of the 'or' gate, signal inversion takes place and an output inverter is needed to restore polarity. Denoting the two signal levels by 0 and 1 as before, Table 2 shows the outputs C for the four possible combinations of inputs A and B.

TABLE 2

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

The limit to the number of transistors which may be placed in series is set by the saturation voltages of the transistors. The sum of these in a series chain must be such as to maintain succeeding stages in an adequately cut off condition. Hence the maximum number is limited to two for reliable operation at 35°C.

The function of the series and parallel configurations may be interchanged if previously inverted signals are available. The results may be expressed in terms of switching algebra[6] as follows:

For negative going inputs of A and B, the parallel configuration forms an output $C = \overline{A + B}$, which becomes $A + B$ on inversion. The series configuration gives an output $C = \overline{AB}$, which after inversion becomes $A.B$. For positive going inputs of $\bar{A}$ and $\bar{B}$, the parallel configuration forms an output $C = \overline{\bar{A} + \bar{B}}$, and the series configuration forms an output $C = \overline{\bar{A}.\bar{B}}$.

Since $A + B = \overline{\bar{A}.\bar{B}}$. and $A.B. = \overline{\bar{A} + \bar{B}}$, each configuration has an equivalent in terms of the other as shown in Fig.5c.

2.4 The directly coupled bistable

If two inverter amplifiers are mutually coupled as illustrated in Fig.6, an element known as the bistable is obtained. It is given this name because of the fact that it possesses two stable states. If either transistor is conducting, the other is maintained in the cut-off condition and vice versa, thus the outputs can be considered to be in opposite states. In order to cause these states to interchange, it is necessary to short-circuit the transistor which is non-conducting. This need only be done for a period long enough for the device to complete the transition. Having been triggered in this way into one of its stable states, the element will remain thus indefinitely and hence has the capability of information storage.

Inverters or gates as described in the two previous subsections can be utilised to provide the short-circuit triggering function. The collector resistors normally associated with these elements become redundant, since each triggering element and one half of the bistable can share a common load resistor.

The transition time will vary with the number of externally connected transistors that the bistable is called upon to drive and decreases as the number increases[4]. A worst case value, i.e. no external load, is 110 nanosecs.

2.5 Summary of DCTL features

The simplicity of the DCTL technique and the resulting economy in terms of development time, are its main advantages. A complete logic system can be formulated using the elements described in the foregoing and such systems have proved reliable in practice[7]. The minimal use of components other than transistors achieves a degree of compactness which approaches the ideal for this type of construction.

A figure of merit for a circuit element to be used in a logic system is its fan-out figure, i.e. the number of other elements it is capable of driving. Since the transistors possess a relatively high gain at low levels, it might be concluded that the fan-out figure approaches the current gain of the transistor, as the load is composed of multi-base-emitter junctions. The spread of the input characteristic however, prevents this ideal being realised. With reference to Fig.2a, it can be seen that dissimilar transistors will draw different currents at a given value of Vbe. For example at -0.3V a batch of transistors in parallel may draw currents ranging from 0.25 to 0.55 mA. Hence the total current that a batch of transistors will draw is unpredictable. It is necessary therefore to cater for the worst case, which is one transistor whose input characteristic is that represented by the maximum curve in Fig.2a, in parallel with n transistors whose characteristics are represented by the minimum curve. This feature of unequal base current sharing limits the fan-out figure to four and is the most unfortunate aspect of the DCTL technique. It considerably increases the required current demand capability of the timing pulse generator outputs, since these are also required to supply many transistor inputs in parallel.

A further disadvantage is that of the limited maximum operating temperature. The transistors operating in a system of DCTL tend to have relatively high leakage currents in the rather nebulous cut-off condition. Since this current doubles per 10°C temperature rise, a temperature is soon reached where the leakage current in the associated collector resistor begins to severely limit the current flowing to succeeding transistor bases. Hence for a fan-out figure of four, the maximum operating temperature is limited to 35°C. This means that the timing pulse generators need not operate above this level, which in turn increases their permitted fan-out figure.

3 THE p PULSE SYSTEM

3.1 The p pulse generator

This generator has been designed to produce four interleaved pulse trains all operating at the 1 Mc/s rate and having equiduration pulses (see Fig.1). It is composed of three main elements, the basic clock, cyclic binary counter and pulse divider, which are described in the ensuing subsections.

3.1.1 The basic clock

The function of the clock is to provide an accurate frequency standard to serve as the basic waveform from which all others are derived. It is made up of three stages, the first two using alloy junction transistors connected in the common collector configuration, the remaining one using a surface barrier transistor operating in the common emitter mode. A schematic diagram is shown in Fig.7. The first stage is a crystal controlled 2 Mc/s oscillator which has a quartz crystal in the base circuit and a resistive-capacitive load. The device depends for its operation upon the fact that a grounded collector amplifier with a sufficiently capacitive load, presents a negative resistance component at its input terminals. Thus oscillations can be maintained across the load and if the voltage developed across the crystal stabilising capacitor in the base circuit is utilised, an output waveform of exceptional purity and stability is the result. The following stage acts as a buffer, protecting the oscillator from the effects of a varying external load impedance.

The remaining stage converts the sinusoidal output waveform to a square wave at the same frequency. The negative-going portion of the sine wave switches the transistor on, its base current being supplied by the buffer amplifier. The germanium OA47 diode simulates the base-emitter junction of the surface barrier transistor and draws a current practically equal in magnitude to that of the base during the period of the positive-going portion of the wave. Thus currents equal in magnitude but opposite in direction flow during the two halves of the periodic time, ensuring equality of the output mark to space ratio.

3.1.2 The cyclic binary counter

Digital counting can be performed using bistable elements in conjunction with 'and' gates. If a number of bistables are triggered in a cyclic sequence, then by suitable gating of the resultant output waveforms, any periodic time or 'mark' period of the triggering waveform within the cycle can be defined.

The duration of this cycle is dependent upon the number of bistable elements. Since each bistable possesses two inputs, then n elements have 2^n possible states. This means that a maximum of 2^n interleaved pulse trains having equiduration pulses can be generated within a cycle period.

The bistables may be switched in any convenient order through their 2^n states and in this case they are switched according to the Gray code. An example of the latter for two variables A and B is given in Table 3.

TABLE 3

A	B
0	0
0	1
1	1
1	0

The salient feature of this code is that only one variable changes in going from any one state to the next. This characteristic is useful in this application, since it means that the time delay between the application of a trigger pulse to a bistable and the production of the corresponding output transient is virtually constant for every change of state.

The description of the way in which the correct switching sequence was obtained in this case is aided by reference to Fig.8a, which shows the logic diagram of the cyclic binary counter. Since four output waveforms are required, two bistables are needed. The associated 'and' gates steer the incoming clock square wave in such a way as to cause one bistable to change state during the 'mark' period and the other during the 'space' period. To achieve this end, phase inversion of the clock signal to one of the bistables must be performed and this is provided by the inverter element.

The outputs of each bistable are used to provide reference states for routing the clock signal to the other. Thus each bistable controls the triggering of it's counterpart, suitable cross-connections ensuring that the output sequence follows Table 3 above.

The appropriate connection to any given steering gate can be determined by considering the required triggering signals for its associated half-bistable. The latter must be in the 'off' or 1 state immediately prior to switching and then it must be ensured that the polarity of the applied steering pulse is such as to enable the gate to trigger the bistable on the arrival of the clock pulse. The waveforms obtained at the four outputs are shown with that of the incoming clock signal in Fig.8b.

The logic described above is implemented by the use of directly coupled elements as shown in Fig.8c. In the interests of economy, each pair of gates shares a transistor. This is permissible provided that the common transistor

is placed at the bottom of the series chain. It can be seen that the clock signal to the second bistable is phase inverted twice instead of being routed directly to the gate. This was done to avoid the possible instability which would be brought about by the effects of two varying loads on the clock waveform.

3.1.3 The pulse divider

The pulses generated by the cyclic binary counter have the same repetition frequency, but have a duration which is double that required of the p pulses. This can be remedied by gating suitable pairs of output waveforms, this being the function of the pulse divider.

The gating is performed using directly coupled elements. Since both input polarities are available, a choice exists between the series and parallel type of configuration. As the latter provides a superior '0' or 'on' level, this type was chosen. Table 4 below shows both outputs of bistables A and B over one cycle and the inputs to the gates for a given output may be selected by reference to it. They are:-

TABLE 4

$$p_1 = A.B. = \overline{\bar{A} + \bar{B}}$$

$$p_2 = A.\bar{B}. = \overline{\bar{A} + B}$$

$$p_3 = \bar{A}.\bar{B}. = \overline{A + B}$$

$$p_4 = \bar{A}.B. = \overline{A + \bar{B}}$$

A	$\bar{A}$	B	$\bar{B}$
1	0	1	0
1	0	0	1
0	1	0	1
0	1	1	0

A circuit diagram showing input and output variables is given in Fig.9.

3.2 The p pulse amplifiers

The outputs of the pulse divider are each capable of driving four other directly coupled elements. To increase the effective fan-out figure, these four elements could be made to be inverters each driving four others. The fan-out figure is thus increased to 16 for each pulse, but the double inversion involved allows the position in time of the output leading edge to be influenced by the effects of hole storage. The spread in the hole storage factor for the SB 240 is such that the displacement in time between the leading edges of the outputs from transistors amplifying the same pulse could be as large as 25 nanoseconds. This is intolerable since this figure represents 10% of the output pulse width. Hence the need existed for a high frequency high gain pulse amplification system. The transistor to be used in such a system needs to embody the following characteristics:

(1) High current gain at large current levels.

(2) A high cut-off frequency.

(3) A low hole storage factor.

(4) A low collector saturation voltage.

A transistor which well meets the first three of these requirements and which is readily available is the ASZ21. This is a germanium junction transistor of the p.n.p. alloy diffused type manufactured by Mullard Ltd. It features a typical current gain at Vce = -1V, Ic = 30 mA, of 75 and a minimum cut-off frequency (f_1) of 300 Mc/s. The manufacturers do not express the effect of hole storage in terms of a hole storage factor, but experiment indicates a maximum value of 40 nanosecs. The only undesirable feature of this transistor is its relatively high collector saturation voltage (-0.7 typical, -1.2V max. at Ic = 50 mA, Ib = 3 mA). Hence if the effects of this can be eliminated the transistor is suitable for use in the application outlined above.

The circuit arrangement of a pulse amplifier designed around the ASZ21 transistor is shown in Fig.10. It consists basically of two stages both connected in the common emitter configuration. The first is coupled to the pulse divider by the network C1 R2 and R3. The values of R2 and R3 are chosen so that the base of VT1 is held positive with respect to the emitter in the cut-off state, whilst allowing the relative values of R1, R2 and R3 to supply the minimum base current for collector saturation in the 'on' state. C1 provides a path for input current overdrive during both switching transients. Considering the turn-on of VT1, the initial input current is the sum of two components, one through R2 which is constant, the other through C1 which is initially high then decays exponentially. During the period of the pulse, C1 is allowed to charge fully to the voltage drop across R2 and the base current falls to the minimum value for saturation. Hence at a time immediately prior to turn-off, the charge stored in the base region is at a minimum. During the turn-off transient, the charge stored in the capacitor acts to neutralise that stored in the base, the positive current in R3 assisting in this. Thus the transistor is overdriven in both directions, this having the effect of reducing both the turn-on and turn-off delay times. In general, a current overdrive factor beyond 4 to 1 produces very little improvement in delay time.

Consider now the output stage. The maximum number of paralleled surface barrier transistors which it can be called upon to drive is governed by the effect of the hole storage charge of these transistors, encountered when VT2 comes into conduction. The turn-on time of this transistor is considerably lengthened by this effect, which is such as to cause current to be shunted away from the transistor to neutralise the stored charge, thus delaying the completion of switching. Hence the transistor in the load with the greatest hole storage factor will dictate the duration of the turn-on time, which in the worst case, could be equal to the period of the pulse. Another problem is that of the relatively high collector saturation voltage of the output transistor. Unless the latter is saturated heavily thus forfeiting its high current gain, the load transistors will remain in conduction for both switched states.

These two difficulties are overcome by placing a source of positive current in the emitter leg of the output transistor. This source is controlled by the components R7, R8 and C3. The values of R7 and R8 are chosen so as to limit the emitter potential to a convenient level during the cut-off state of VT2.

At the same time however, the relative values of R6, R7 and R8 have to be such as to allow a current to flow in VT2 in its 'on' state of sufficient magnitude to drop all of the collector supply voltage across R6. This can be taken a stage further by increasing this current so as to allow R6 to develop slightly more than the supply voltage across it. This has the advantage of reducing the leakage current in the load transistors to Icoo (base-emitter reverse biased) which in this case is an almost negligible value. The value of C3 is made such that the charge stored in it during the cut-off state of VT2, is sufficient to neutralise the charge stored in the base regions of the load transistors when VT2 is turned on. The fan-out figure of the output stage with the supply voltages available was found to be 15.

VT1 drives VT2 via a RC coupling network. VT2 is maintained in conduction during the cut-off period of VT1 by the current flowing in R5 from the supply rail. When VT1 is caused to conduct, the positive going excursion at its collector is transmitted wholly to the base of VT2. This is brought about by selecting the values of R4, R5 and C2 so that their time constant is large compared to the period of the pulse. This relatively large excursion switches VT2 off and allows the emitter potential of VT2 also to rise to a comparatively high level. This sets the level to which C3 can charge in readiness to fulfil its function of reducing the turn-on time.

The loss of current gain and the increased turn off time associated with the use of heavy saturation to reduce the inherently high bottoming voltage of the transistor used, is avoided by the use of the couplings described above. Thus the fan-out figures of both stages are kept to a maximum. The first stage is capable of driving twelve output stages, which means that each p pulse amplifier is capable of supplying 180 surface barrier transistors. A block diagram of the p pulse system is given in Fig.11.

In brief, the performance figures are: output rise and fall times over 0.5V - approximately 15 nanosecs, overall delay time 15 nanosecs, difference between the leading edges of the pulses from twelve output stages in parallel not more than 5 nanosecs.

4 THE P PULSE GENERATOR

4.1 General description

The P pulses are generated using the same technique as for the p pulses. Since the Gray code is unwieldy to implement when the number of variables n is greater than 2, an alternative switching sequence is used which gives rise to a few differences. Another departure from the previous case arises because of the fact that 25 P pulses are required, a number which lies between 2^4 and 2^5. Thus five bistables must be used and their switching sequence stopped after 25 by resetting the counter instantaneously to the start condition.

The sequence which is simplest to implement is that of the binary code, because by using complementing bistables, the trigger pulse for each bistable after the first can be derived directly from its predecessor. By triggering the first bistable with p_1, the resulting output waveforms are synchronised with the p pulses. The binary sequence for five variables A, B, C, D, and E where A is the least significant is shown in Table 5.

TABLE 5

A	B	C	D	E
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	1
1	0	0	1	1
0	1	0	1	1
1	1	0	1	1
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

It can be seen from this that whenever a bistable is to change its state, its predecessor must also change its state from 1 to 0. This feature of the code can be exploited to generate the required trigger pulse. Assuming that the latter is generated in this way and that the sequence begins at 00000, a difficulty is encountered when the counter is reset. If any bistable is reset from 1 to 0, it will propagate a trigger pulse to its successor. This situation is prevented from arising by starting the sequence at 11111.

It can be seen by further examination of Table 5, that the number of bistables which change state at each transition varies from 1 to 5. Moreover, the trigger pulse propagation is serial, i.e. each bistable must change its state before it can propagate a trigger pulse to the next. Thus the time required for the completion of each transition is not constant and this gives rise to P pulses of insufficient and differing durations.

The problem of the differing pulse durations can be solved if the bistables can be made to change state simultaneously at each transition. Referring to Table 5, it can be seen that whenever any bistable except the first in a row is to change its state in either direction at the next transition, all its predecessors are in the '1' state. This fact is the basis of the design of a parallel trigger pulse transfer network, which equalises the transitional time delay.

This delay, although constant, is also undesirable since the output P pulses will be deficient in duration by the same amount. It can be eliminated by triggering the first bistable with p_4 via a delay network, which has a delay time equal to the period of a p pulse minus the transitional time delay. The P pulses generated in this way are thus accurately aligned at their leading edges with that of p_1. Their trailing edges will be similarly aligned with that of p_4 if the turn-on time of the transistors used is small.

The P pulse generator is thus seen to consist of four main elements; a binary counter, a pulse dividing gate matrix with its associated output amplifiers and a parallel trigger pulse transfer network. The design of the reset network is such as to incorporate that of the transitional delay elimination, which gives rise to the fourth main element. These elements, apart from the reset network, were designed around the ASZ21 transistor and are described in the following sub-sections.

4.2 The binary counter

The binary counter consists of five complementing bistables, so called because after each trigger pulse to an input line common to both sides, either output signal represents a '1's complement of its previous value. The common input line is made possible by alternate routing of the input pulse by each half of the bistable to the other. This is accomplished by connecting a resistor-capacitor-diode gate to each half of a resistance coupled bistable in the manner described below.

4.2.1 The resistance-coupled bistable

This type of bistable utilises potential divider networks as a means of cross coupling the two transistors as shown in Fig.12a. The value of R1 must be such as to supply the current required by the external load in the cut off state of its associated transistor, plus the minimum base current for saturation of the other. When either transistor is conducting, the associated values of R2 and R3 must be such as to reverse bias the emitter-base junction of the other transistor (suffix a when VT1 conducts, b for VT2) 01 provides for input current overdrive in both directions in the manner described in section 3.2. ASZ21 transistors are used for three reasons (a) they exhibit very little hole storage in this circuit, (b) their fast switching speed and (c) they are capable of switching a current large enough to drive the ensuing pulse dividing gates directly.

The bistable as it stands however has one drawback. Although the '0' level is sufficiently well defined by the saturation voltage of the transistors, the '1' level depends upon the value of the external load. This drawback is eliminated by suitably increasing the collector supply voltage and connecting

a diode, which is referred to a supply voltage equal to that of the desired '1' level, to each collector. The additional components are shown in dotted form. Now when either transistor is driven towards cut-off, its collector potential falls towards V1 but is clamped at V2 by the diode coming into conduction at this level. The load current is thus shunted into the diode and the latter acts as a current reservoir, whilst maintaining constant voltage. Thus the outputs are made to present a low impedance in both states at well defined levels.

4.2.2 The resistor-capacitor-diode gate

The function of this element is to produce an output at the coincidence of a pulse type signal with a steady state signal. Consider the circuit of Fig.12b. The steady state signal can be in either of two states 0 and 1 at voltage levels E_0 and E_1 respectively and is applied to the resistor. The positive-going pulse signal is applied to the capacitor. If the load circuit is such as to maintain the output level at E_0, then when the input line to the resistor is at a level E_1 (negative with respect to E_0) the diode is reverse biased. Then if a positive-going pulse having an amplitude equal to that between the limits E_0 and E_1 is applied to the capacitor it will have no effect. If the input to the resistor is made E_0 however, the diode is unbiased and a positive-going pulse applied to the capacitor will appear at the output line.

4.2.3 The complementing bistable

A complementing bistable can be formed using a resistance-coupled bistable in conjunction with two resistor capacitor diode gates in the manner shown in Fig.12c. The diodes of the two gates are connected to the bases of the transistors, the resistors to the collectors and the capacitors are linked to form a common input line. Assume initially that VT1 is conducting and that VT2 is cut off. Both collector and base of VT1 will be at small negative potentials such that D1a is slightly forward biased. C1a is charged to a potential practically equal to the difference between the two collector potentials, this being almost equal to the input signal amplitude. The collector of VT2 will be at -V2 and the base at a slightly positive potential. Thus D1b is reverse biased to an extent practically equal to the difference between the two collector potentials and C1b is uncharged.

A positive-going pulse applied to the input line will be routed through D1a since it is forward biased. C1a rapidly discharges to the difference in potential across it via the base-emitter junction of VT1 at one end and a bottomed transistor at the other. C1b begins to charge, but the time constant C1b R1b is too large for this to be of any consequence. The pulse routed to VT1 base causes VT1 to switch off, resulting in a change of state. D1a becomes reverse biased and C1a begins to re-charge slowly with a time constant C1a R1a. The two ends of the branch formed by C1b and R1b in series are now at the same potential and C1b loses the small charge acquired prior to and during the change of state. This however is too small to effect re-triggering of the bistable whilst the input pulse is present. When the latter is removed, C1a returns the small charge acquired during the period of the input pulse. C1b now has to become charged to a potential equal to the input pulse amplitude and will do so in approximately 3C1b R1b seconds. Hence no further input signals can be

applied until this process is complete. This sets the upper limit to the repetition rate at which the bistable may operate. The next input pulse will reset the bistable to its initial state in the same way as before, the above description being valid if suffix a and b are interchanged.

4.3 The parallel trigger pulse propagation network

The need for the application of a trigger pulse to a bistable at any transition can be detected by inspection of the states of its predecessors immediately prior to the transition. These states will all be 1's as described in section 4.1. Therefore the states of the bistables preceding any given bistable are applied to an 'and' gate and compared to the incoming trigger pulse. If this is done for each bistable, then the elements which are required to change state at each transition will do so simultaneously. Since the bistables change state immediately upon the receipt of a pulse, the states applied to the gates must be delayed for the period of this pulse. The logical diagram of the resulting parallel transfer binary counter is shown in Fig.13a.

The circuit arrangement for the logic between bistables A and B only is shown in Fig.13b, the others being similar. The required delay is obtained using lumped parameter delay networks[8], comprising ten pi network LC sections to obtain the required bandwidth. The gates used are of the resistance rectifier type an example of which is shown in Fig.14a. This shows a circuit element comprising two diodes and a resistor and its action can be described as follows:

In the quiescent state, both input levels are equal and the current that flows in R maintains the output level equal to that of the input minus the negligible voltage drop across the diodes. If a positive-going signal is applied to one diode only, it becomes reverse-biased. This occurs because the other diode is able to maintain the output line at practically the same level as before, provided that its source impedance and its forward resistance are both low. If positive-going signals are applied to both diodes simultaneously the output level must rise correspondingly. Hence this element is seen to be an 'and' gate for positive-going signals. The conditions for optimum response from this type of gate are that the signal excursion should be small compared to the supply voltage and that the source impedances should be low in both states. In addition, the value of R should be high compared to the forward resistance of the diode used and low compared to the diodes inverse resistance. The 'and' gate components in Fig.13b are those represented by D2, D3 and R4. The gate inputs are driven by common emitter stages centred around VT1 and VT2. A common collector stage designed around VT3 matches the output resistance of the gate to that of the following bistable input.

In the quiescent condition VT1 is cut-off and the base potential of VT3 is limited by its collector-base diode which is conducting in the forward direction. Since the output of VT1 supplies an input to all the gates, they are thus held closed regardless of the states of the bistables. VT3 is thus caused to conduct, its output line assuming a potential practically equal to the collector supply voltage and diode D5 is thus reverse biased. If the input from bistable A is in the quiescent or '0' state, VT2 must be held in the non-conducting state. This is ensured by the current flowing in R2, R1

and D1, which maintains the base potential more positive than that at the emitter. D.C. isolation between the bistable and VT2 is necessary because of the dissimilar levels at which they operate and is effected by capacitor C1.

If bistable A output is in the '1' state however, VT2 must be made to conduct. The coupling between these stages is of the RC type, the resistive component being the input resistance of the VT2 stage. In this state, diode D1 is reverse biased and since R2 is large compared to R1, the input resistance is determined mainly by the sum of R1 and the dynamic slope resistance of VT2 base-emitter junction. The delay line is inserted between the bistable and VT2 stage and to obtain correct matching, its characteristic impedance which is almost purely resistive, is made equal to an approximate value for this input resistance. Consider now a point in time where a trigger pulse arrives when bistable A is in the '1' state and is about to change states. Reference to Table 5 shows that whenever these conditions exist, bistable B must also change its state. The delay network will maintain VT2 in the conducting state for the period of the trigger pulse. Thus both VT1 and VT2 conduct and the gate is opened. The current flowing in R4, D4, D2 and D3 establishes a potential at VT3 base which is more positive than that at the emitter, due to the current flowing in R5 and D5. The voltage drop across diode D4 is needed to establish the above condition, this being the diode's only function. Thus VT3 is cut-off for the period of the trigger pulse and the resulting positive-going output is applied to bistable B input, causing it to change its state. A diagram showing the phase relationship between the relevant waveforms for the circuit action described above is shown in Fig.14b. All the remaining delay network and gate circuits function in the same way and thus all bistables which are required to change state at any transition do so simultaneously upon the arrival of the trigger pulse.

4.4 The pulse dividing and amplification network

It is the function of this network to select and amplify 25 consecutive combinations of 5 variables out of the possible 32 as illustrated in Fig.15. The output amplifiers are required to drive surface barrier transistors and have a specification similar to that of the p pulse amplifiers (section 3.2).

4.4.1 The diode matrix

The selection of the P pulses can be carried out using 'and' gates of the resistance rectifier type in the form of a matrix, an example of which is shown in Fig.16a. This matrix selects the four possible pair combinations of two variables A and B. An examination of the matrix circuit will reveal that it is nothing more than four two-input 'and' gates. This arrangement is easily extended so as to enable it to select from 5 variables. In this case 25 outputs are required, therefore the number of diodes required would be 125.

It is possible however, to carry out this function whilst effecting an economy in the number of diodes used. This is achieved in the following manner. The number of input variables n are grouped in pairs if n is even or in twos and a three if n is odd. The four possible pair combinations of each two variable group are selected using 'and' gates as are the eight possible combinations of three from the three variable group. The groups are then combined using sets

of two-input 'and' gates. In this case subdivision of the variables results in one group of two and one of three. Selecting the maximum number of combinations from the two variable group needs eight diodes, but since only 25 final outputs are required, only seven out of the eight possible combinations are needed from the three variable group, this requiring 21 diodes. Having made these selections, a seven X four array of output lines remain to be combined. Gating 25 pairs of these needs 50 diodes resulting in a total of only 79. This technique suffers from the minor disadvantage that two series diodes appear between each input and output line. The circuit arrangement required to select a P pulse is given in Fig.16b. It is seen that the '0' states of the bistables are selected by the gates, inversion to the negative-going polarity being provided by the output amplifier.

4.4.2 The output amplifiers

These amplifiers are similar in form to and supply the same number of surface barrier transistors as the p pulse amplifiers described in section 3.2. The circuit diagram for a P pulse amplifier is given in Fig.17 and an examination of it shows that the main difference lies in the method by which it is coupled to the pulse dividing gates. The base circuit is similar to that of the gate of Fig.16b, except for the fact that the gate resistor is split into two parts R1 and R2. This facilitates the setting up of the required d.c. bias conditions for VT1. The rest of the amplifier is a facsimile of that of the p pulses except for the diodes D8 and D9, whose function will be described later.

In the steady state, at least one of the bistables connected to the gate diodes D1 to D5 will be in the '1' state. Hence each bistable must be capable of maintaining VT1 in conduction. The output level will be held at a few hundred millivolts above earth in the same way as before.

When all gate inputs are at the '0' level the gate is opened. The current which then flows in R2, R1 and the gate diodes to the bistables establishes a potential at the base more positive than that at the emitter due to the current in R4 and R5. C1 provides for transient overdrive in both directions in the manner described in section 3.2. Thus VT1 is maintained in the cut-off state for the period of the selected pulse and in the absence of a load the output level falls to that of the collector supply voltage.

Owing to the nature of the logic system for which these pulses are generated, the load on any P pulse is different, in general, for each of its four subdivisions p_1 to p_4. The load can vary from one to fifteen transistors and in the cases where one or two only are supplied, the combination of VT1 collector supply and R3 is capable of supplying an excessively high base current to them. A means of current regulation is therefore required and is provided by the diodes D8 and D9. At the lowest voltage that can be developed at the base of an SB 240 with the maximum permissible base current, the two series germanium diodes conduct to the extent where the excess current is supplied by them to R3, thus protecting the load transistors. At the minimum base voltage needed to ensure saturation, i.e. minimum full load voltage, the diodes conduct to a negligible extent. Thus any load from one to fifteen transistors may be safely connected to the amplifier. The hole storage characteristic of the diode used is such as to produce negligible distortion of the output waveform.

4.5 The reset and delay elimination network

The purpose of this element is to reset the binary counter after 25 transitions of its component bistables and to eliminate the overall delay. The required count is achieved by establishing two cyclic sources of input pulses. One of these, starting at a time when the counter is in the state 11111, puts out a succession of 24 trigger pulses to the first bistable and to the inputs of the parallel transfer gates (Fig.13a). During the 25th period, this source is inhibited and a single pulse is generated by the other source, which is used to reset all bistables then in the '0' state. Thus the counter is reset to its initial condition and the cycle repeats continuously. The counter transitional delay is eliminated by generating the pulses of both sources with p_4, and delaying them by the period of p_4 minus the overall delay.

The logic diagram for the network is shown in Fig.18a. It consists basically of two 'and' gates G1 and G3 which are controlled by a bistable called a steering bistable, the setting of which is controlled by another 'and' gate G2 and an inverter. The logic cycle is composed of the following sequence of events. Commencing at $P1p_1$ time, the inverter sets the steering bistable to provide an input to G1. At $P1p_4$ time, G1 opens and supplies an input to the delay network. The latter delays this input by an amount such that the final output from the inverter occurs prior to $P2p_1$ by an amount equal to the counter's transitional delay. The output is applied to the first bistable and to the inputs of the parallel trigger pulse transfer gates (Fig.13a). This causes the counter to change its state and P2 is selected and amplified. The network functions in this way for 24 digit periods and thus puts out 24 trigger pulses. The last of these enables P25 to be selected and the reset pulse must be applied in the next period to reset the counter to its starting condition. If Table 5 is examined it is seen that starting from 11111, the 25th state is 11101. This means that the fourth most significant bistable only needs to be triggered. It is seen by an inspection of Fig.20a, that P25 is fed back as an input to G2. Hence at $P25p_2$ time, G2 opens and resets the steering bistable, thus steering an input to G3. At $P25p_4$ time, G3 opens and the resulting output is applied to the ensuing delay network and buffer amplifier. The delay network performs the same function for the reset pulse as the other delay network does for the trigger pulses. The reset pulse is applied direct to the appropriate base circuit of bistable D which then triggers enabling P1 to be selected. At $P1p_1$ time the steering bistable is set and the cycle repeats.

The basic control logic is implemented using directly coupled elements and the delay networks are again of the lumped parameter type. The trigger line inverter operates in the same way as the inverter amplifiers of the parallel trigger pulse propagation network. Thus the inputs to the parallel transfer gates are all derived from identical stages. The circuit diagram of the network is given in Fig.18b.

The buffer amplifier of Fig.18a is simply a common collector stage, this being the most suitable type of drive for the reset line. In the quiescent state, VT12 is held in conduction by the 12V supply via R8, the voltage at the base being limited by the clamping action of the collector-base diode which is conducting in the forward direction. Diodes D2 and D3 are reverse biased, as is D4 which is included to isolate the bias conditions of bistable D base

circuit from those of the buffer amplifier output. Under signal conditions, VT10 and VT11 are caused to conduct and the resultant positive-going excursion is transmitted by the delay network to VT12 base. D2, D3 and D4 are biased into conduction. D3 thus defines VT12 emitter potential and a more positive potential is developed at the base by adding the voltage drop across D2 to that across D3. VT12 is thus maintained in the cut-off state. Since the input resistance of the buffer amplifier is much higher than the characteristic impedance of the delay network, a reflection is generated. This is of no consequence however since at the time of its arrival at VT10 collector, no other pulse is being generated and the reflected energy is absorbed in R8. The positive excursion transmitted by D4 switches bistable D. Relevant waveforms for the function described above along with those of the binary counter are shown in Fig.19. This completes the delineation of the P pulse generator and the complete logic diagram of it is given in Fig.20.

5 THE A PULSE GENERATOR

The design of this generator is based upon the same technique as for the P pulse generator and uses similar circuitry. A logic diagram of the unit is given in Fig.21. This shows that the counter is of the serial trigger pulse propagation type and implements a switching sequence identical with that of the binary code. The first bistable is triggered by P25 delayed by the period of a P pulse minus the counter's overall delay time. Thus the output leading edges appear coincident with those of p_1 and P1. The second bistable is triggered directly from the first.

An inspection of the binary code sequence for two variables shows that the number of variables which change state at each transition is alternately one and two. Hence the transitional delay time varies. However the delay can be approximately equalised for each transition when only two bistables are involved, by making the speed of response of the second greater than the first. This is achieved by using cross-coupling capacitors (C1 Fig.12a) of a larger value for the second bistable. In this way, the need for a parallel trigger pulse transfer gate is avoided.

The circuit arrangement of the generator is shown in Fig.22 and since it is formulated of the same basic elements used in the P pulse generator, needs no explanation.

6 COMPARISON OF COUNTER TECHNIQUES

At the time that design studies for the pulse generators were begun two other methods of frequency division were considered. One of these used bistables to provide the basic waveforms, but switched them in a sequence identical with that of the Gray code. For reasons stated earlier, the counter transitional delays would all be made equal without the use of parallel transfer gates if this method could be mechanised. The pattern formed by the variables which change state in a progression through the sequence is irregular when the number of variables is large however. In consequence, the amount of logic required to select the particular bistable to be triggered at each transition is much greater than that required for the parallel transfer gates. This is quite apart from the consideration of resetting a counter before the end of its natural count, which is made more difficult by the adoption of this technique.

The other method considered was that of using a ring counter. This consists basically of cascaded stages equal in number to the factor by which the input frequency is to be divided, the final output being connected back to the first stage input. Only one stage is in the signal state at any time and when it is switched to the steady state, propagates a trigger pulse to activate the next. This method has a disadvantage when used for this application in that an output from an activated stage is not obtained until the trigger pulse has been removed. As a result of this, the output pulse duration is deficient by an amount equal to the duration of the trigger pulse. As for the other method considered, the amount of equipment required when the division factor is large is greater than that required for the method which was adopted.

7 CONCLUSIONS

The counters and pulse dividers described in this note have been constructed in the laboratory and their performance has been found to be adequate for the requirements of the system in which they are to be used. The device is now undergoing tests and, to date about 500 hours reliable performance has been achieved.

The choice of transistors used has enabled very fast switching times to be achieved (of the order of 15 nanoseconds on full load). The design principles involved are consequently capable of a wide variety of applications in which a precise source of control pulses is required for digital arithmetic operations.

Each output is capable of providing control p pulses to a maximum of 180 locations, but for the particular application envisaged it has not been found necessary to provide such a large "fanning out" factor. It is felt, however, that the only consideration which might prevent this figure being achieved in practice, is that of a suitable earth return path to cope with the high rate of change of current.

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8	Millman, J.M. Taub, H.	Pulse and digital circuits. Chapter 10. McGraw Hill Book Co. Inc.

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FIG. 1.

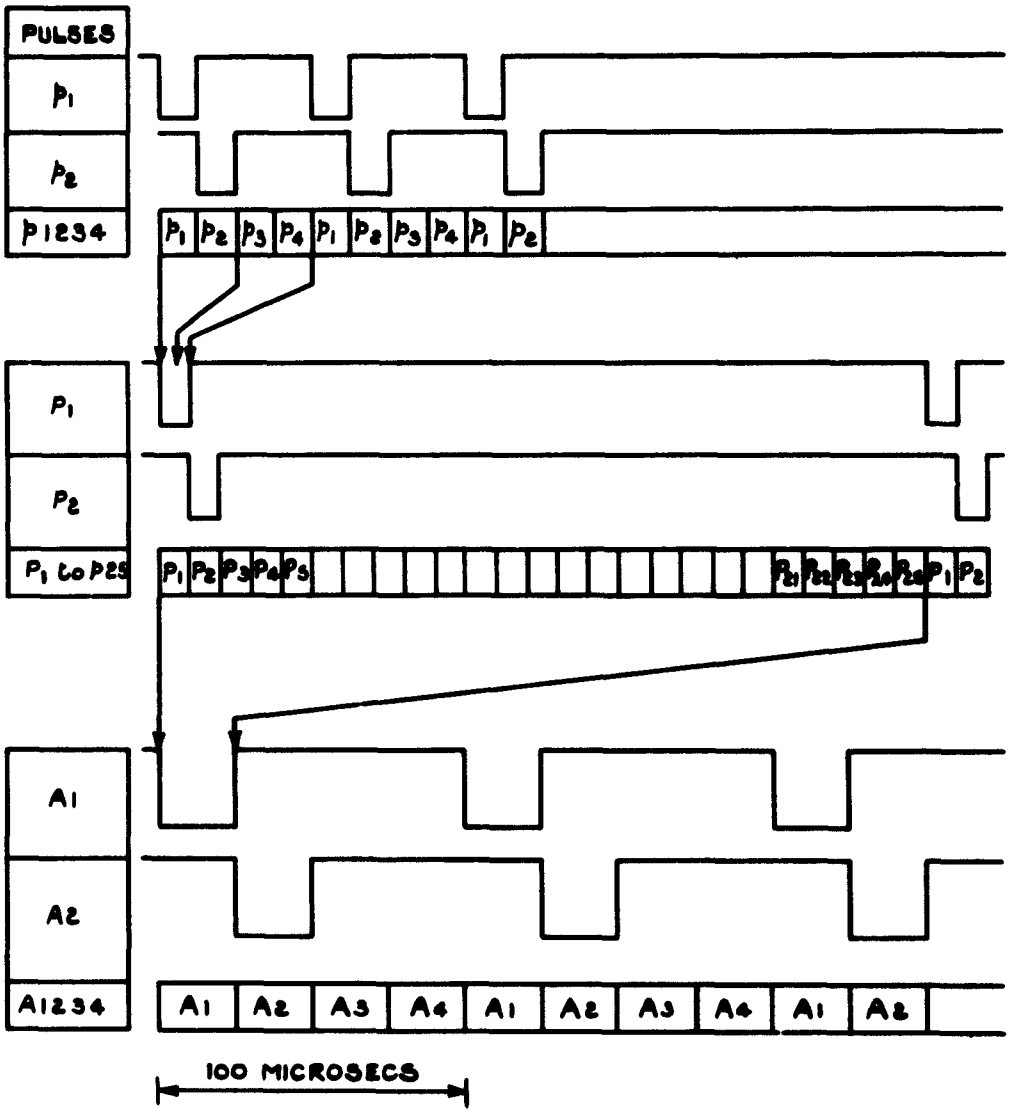


FIG. 1. PHASE RELATIONSHIP BETWEEN TIMING WAVEFORMS.

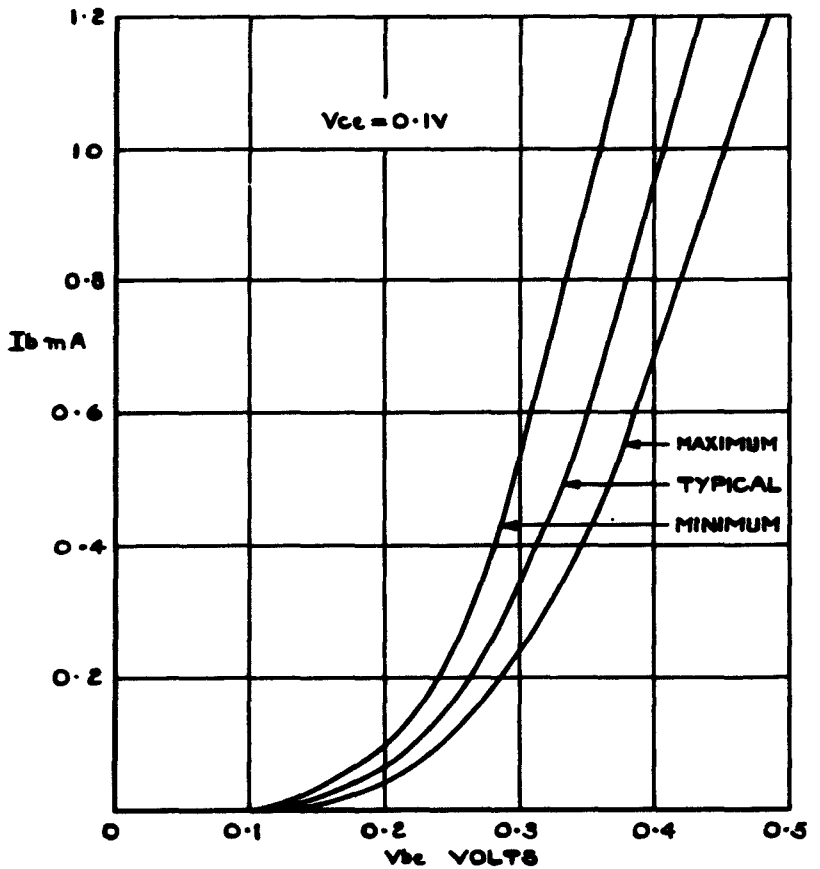


FIG 2(a) SPREAD OF SB240 INPUT CHARACTERISTIC.

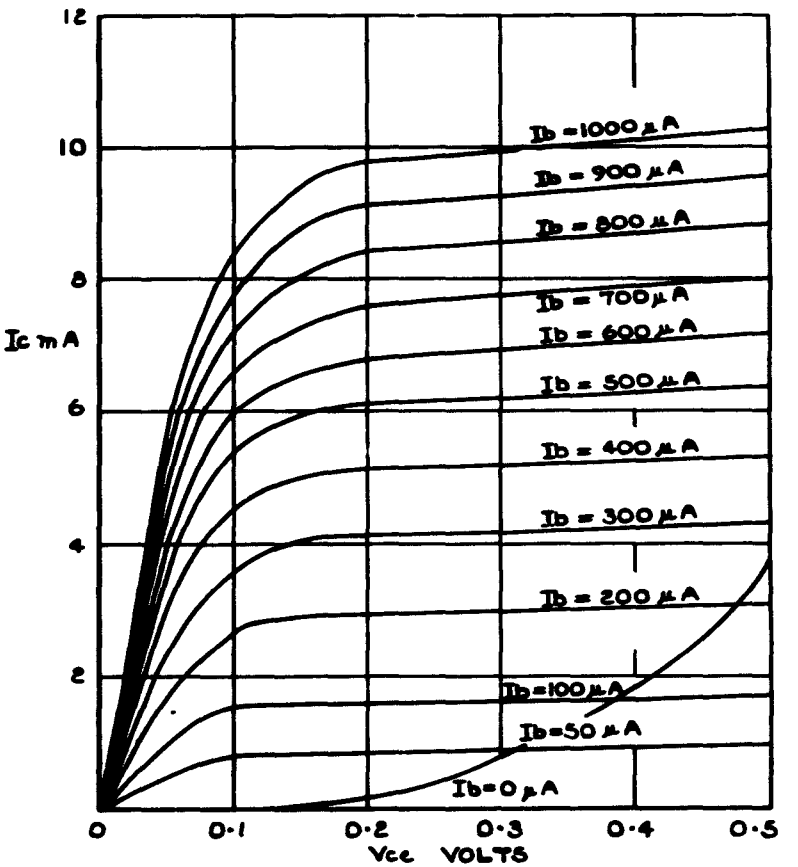


FIG. 2(b) TYPICAL OUTPUT CHARACTERISTIC OF SB240.

FIG. 2 (a & b)

T.N. I.E.E.33

FIG. 3.

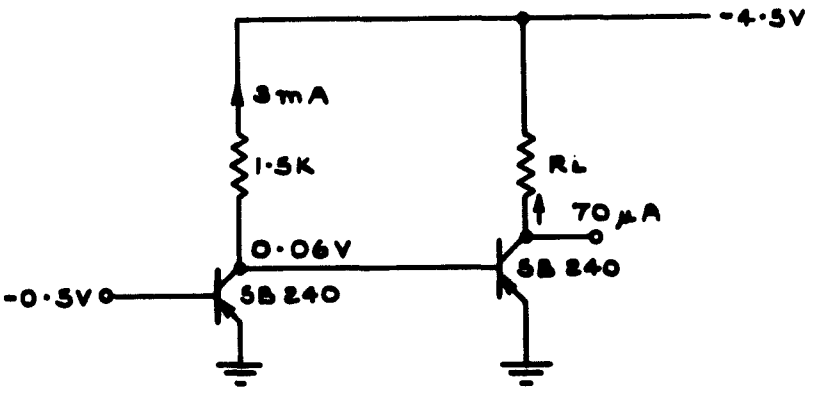


FIG. 3. TYPICAL DIRECTLY COUPLED COMMON EMITTER STAGES.

FIG. 4.

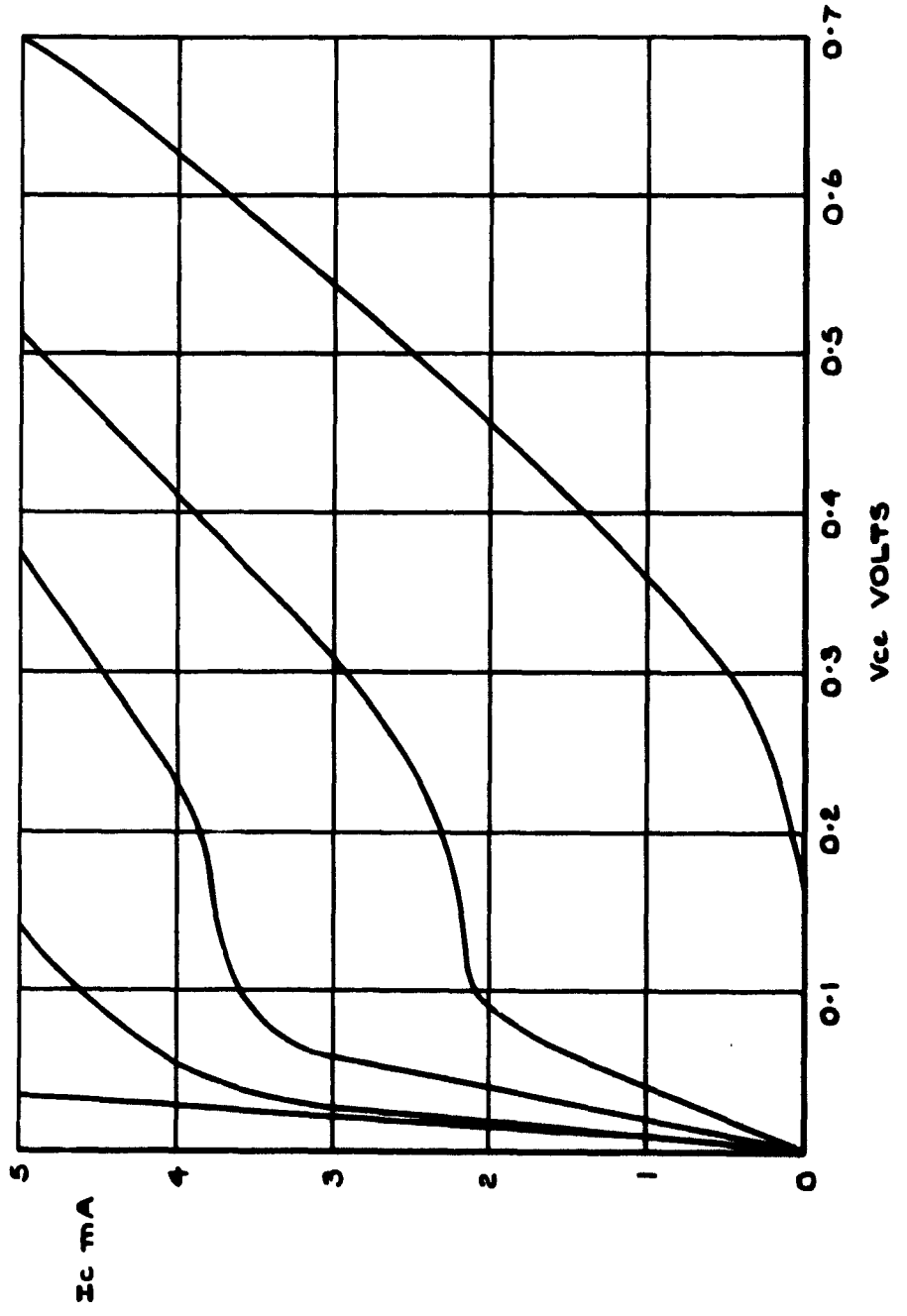


FIG. 4. TYPICAL DIRECTLY COUPLED SB240 OUTPUT CHARACTERISTIC.

FIG. 5.(a–c)

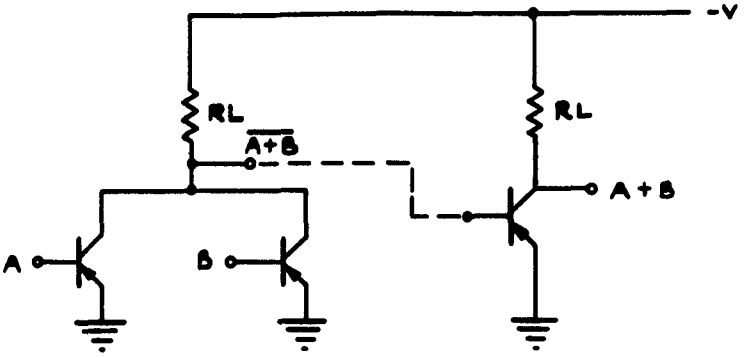


FIG. 5 (a) DIRECTLY COUPLED TRANSISTOR OR GATE.

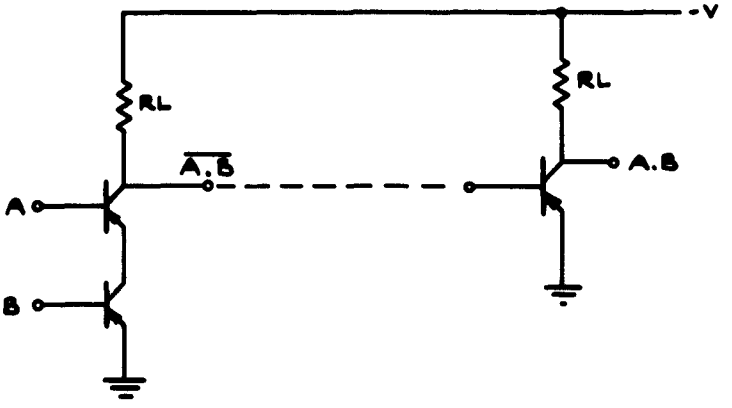


FIG. 5.(b) DIRECTLY COUPLED TRANSISTOR AND GATE.

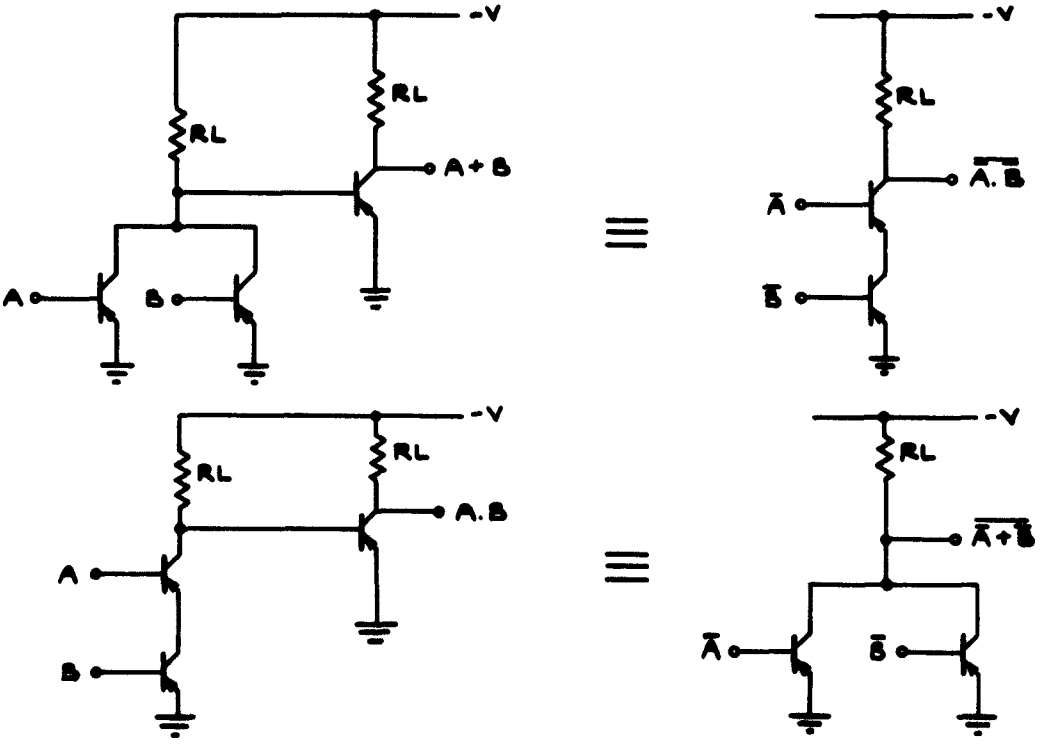


FIG. 5.(c) LOGICAL EQUIVALENTS.

FIG. 6

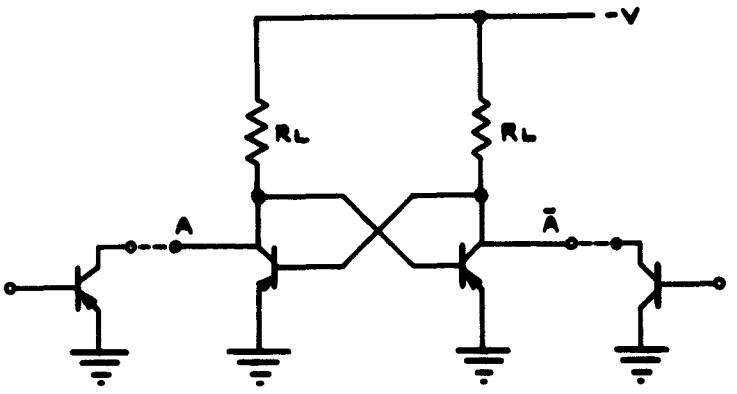


FIG. 6. DIRECTLY COUPLED BISTABLE AND TRIGGERING INVERTERS.

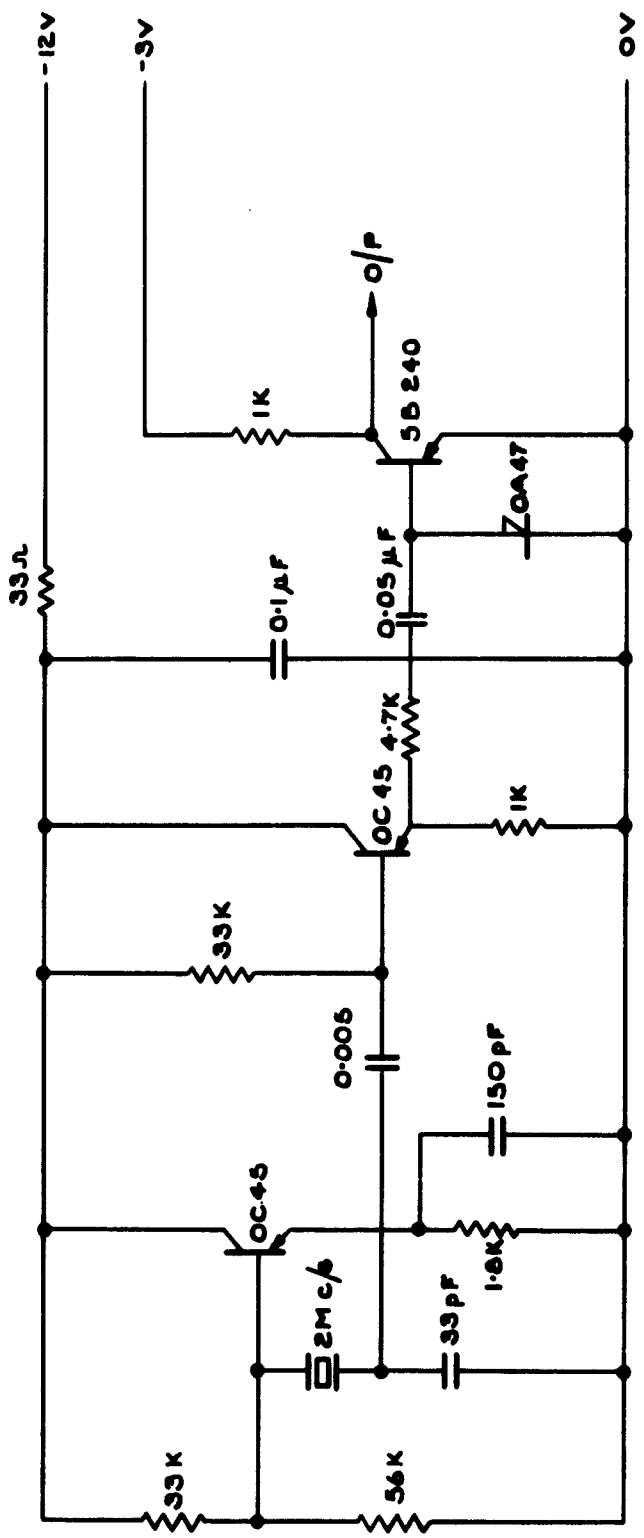


FIG. 7. THE BASIC CLOCK CIRCUIT.

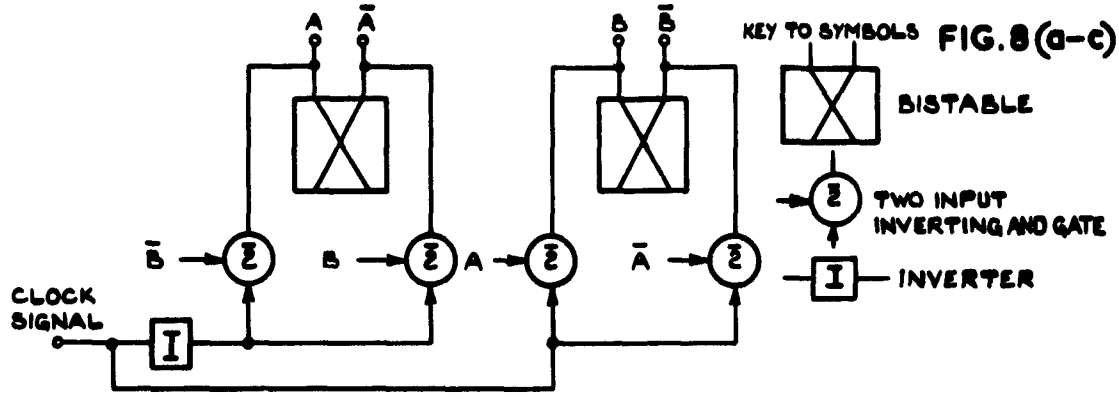


FIG. 8.(a) LOGIC DIAGRAM OF CYCLIC BINARY COUNTER.

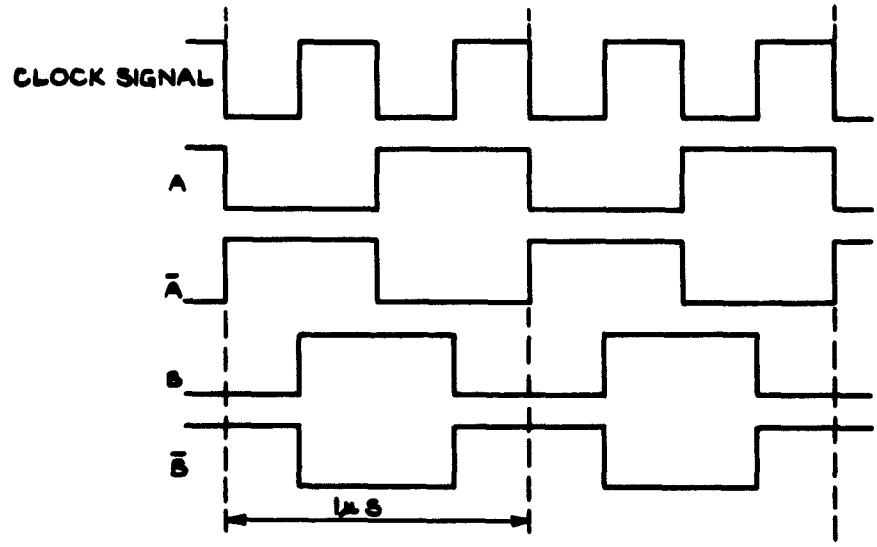


FIG. 8 (b) CLOCK SIGNAL AND OUTPUT WAVEFORMS.

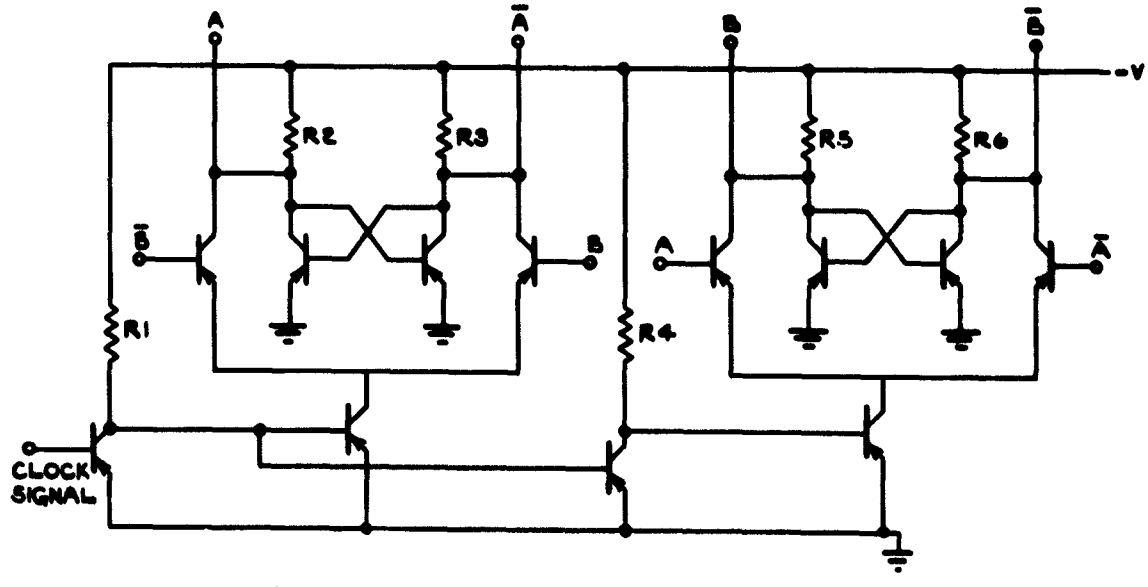


FIG. 8 (c) CYCLIC BINARY COUNTER SCHEMATIC.

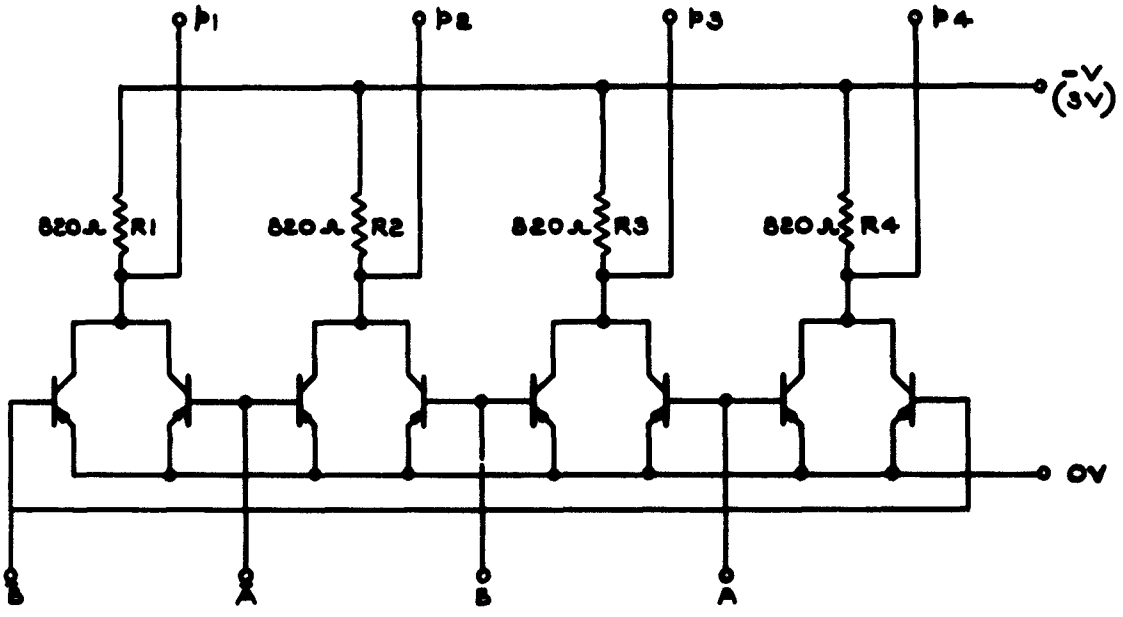


FIG. 9 THE PULSE DIVIDER.

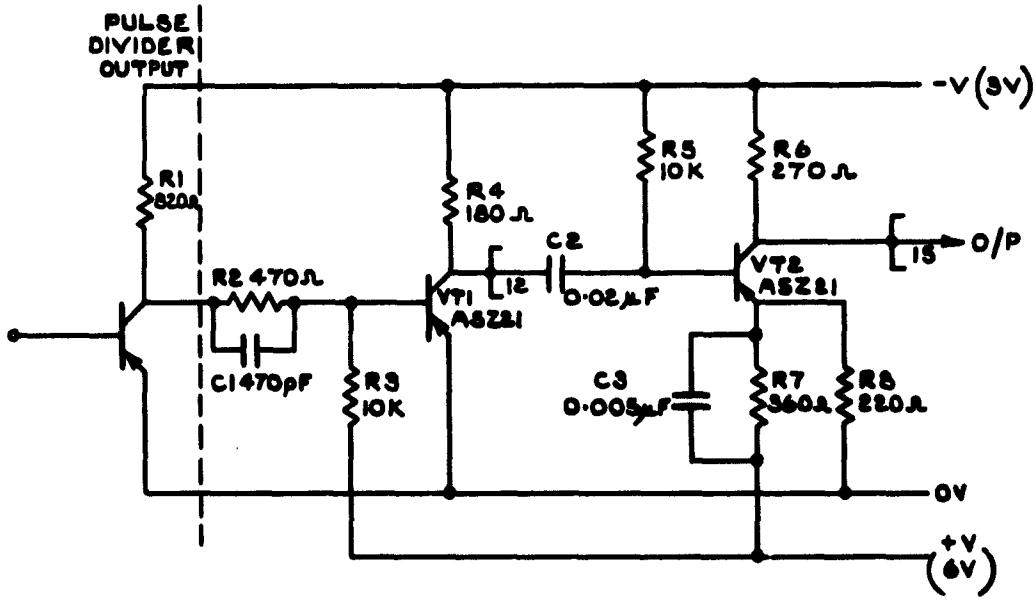


FIG. 10. p PULSE AMPLIFIER.

FIG. 11.

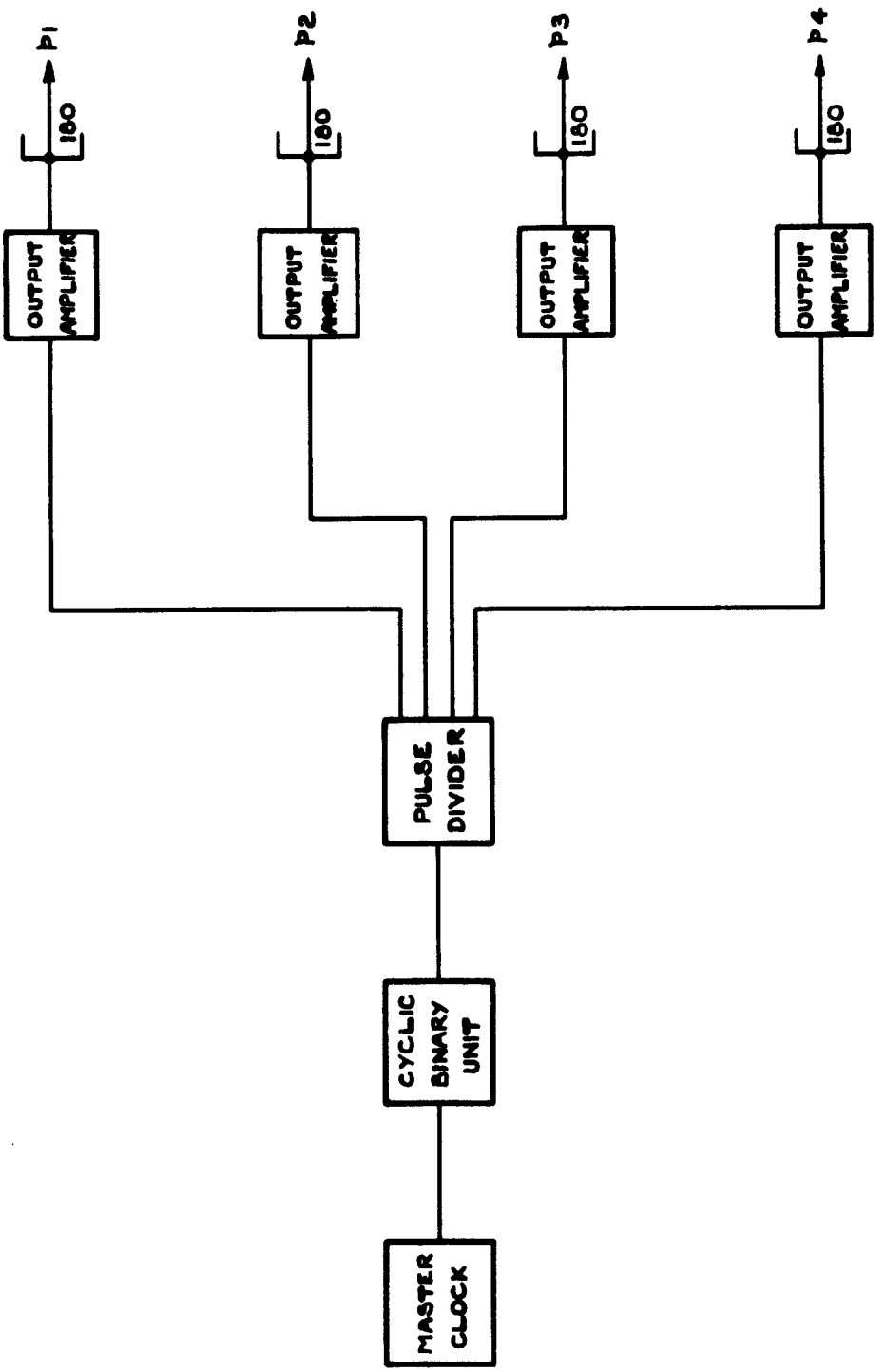


FIG. 11. BLOCK DIAGRAM OF p PULSE SYSTEM.

FIG. 12.(a-c)

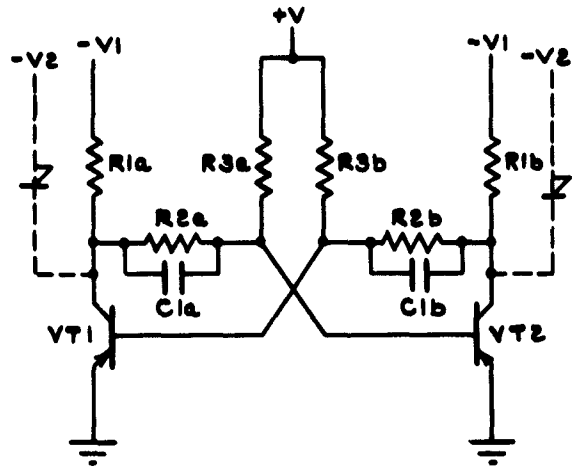


FIG. 12.(a) RESISTANCE COUPLED BISTABLE.

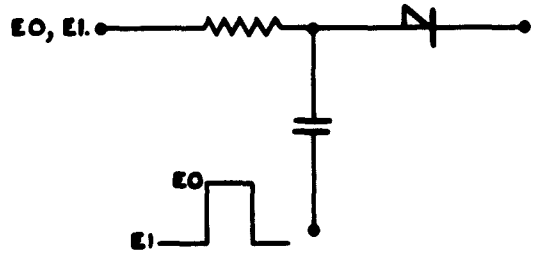


FIG. 12.(b) RESISTOR-CAPACITOR DIODE GATE.

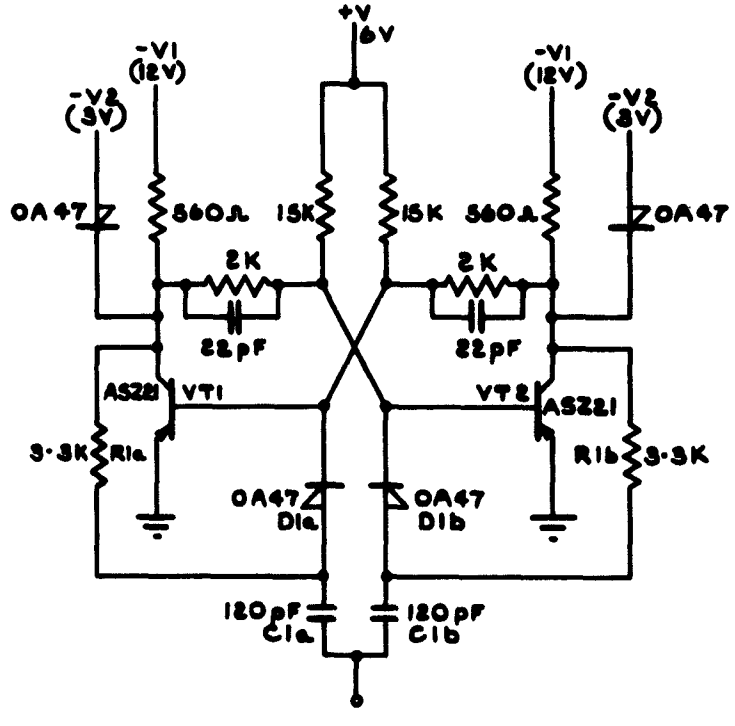


FIG. 12.(c) COMPLEMENTING BISTABLE.

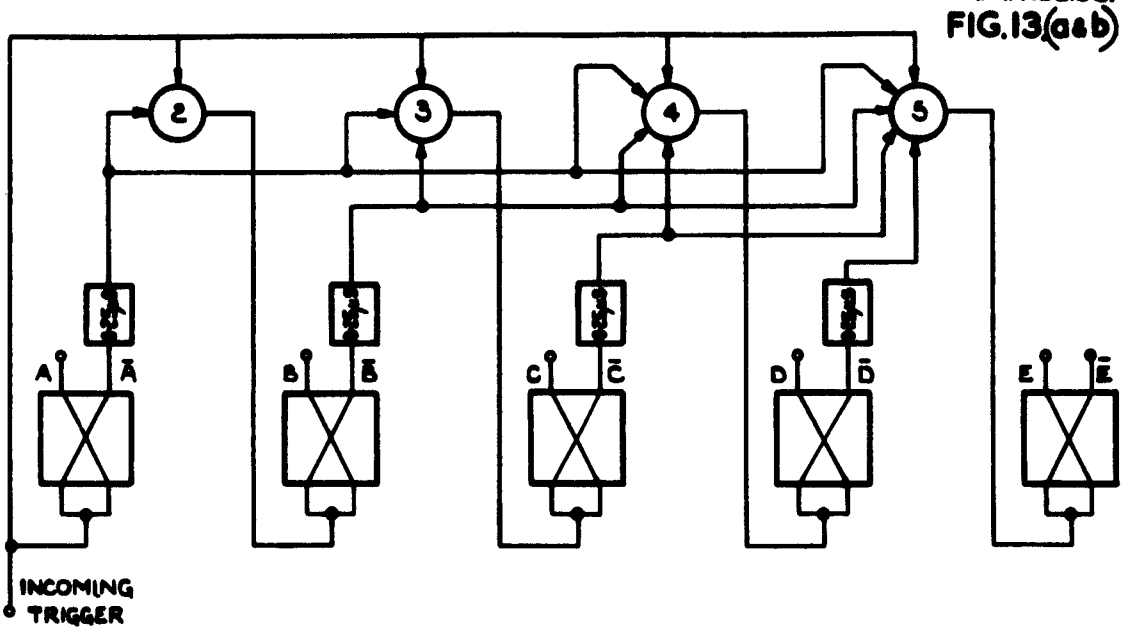


FIG.13.(a) PARALLEL TRANSFER BINARY COUNTER.

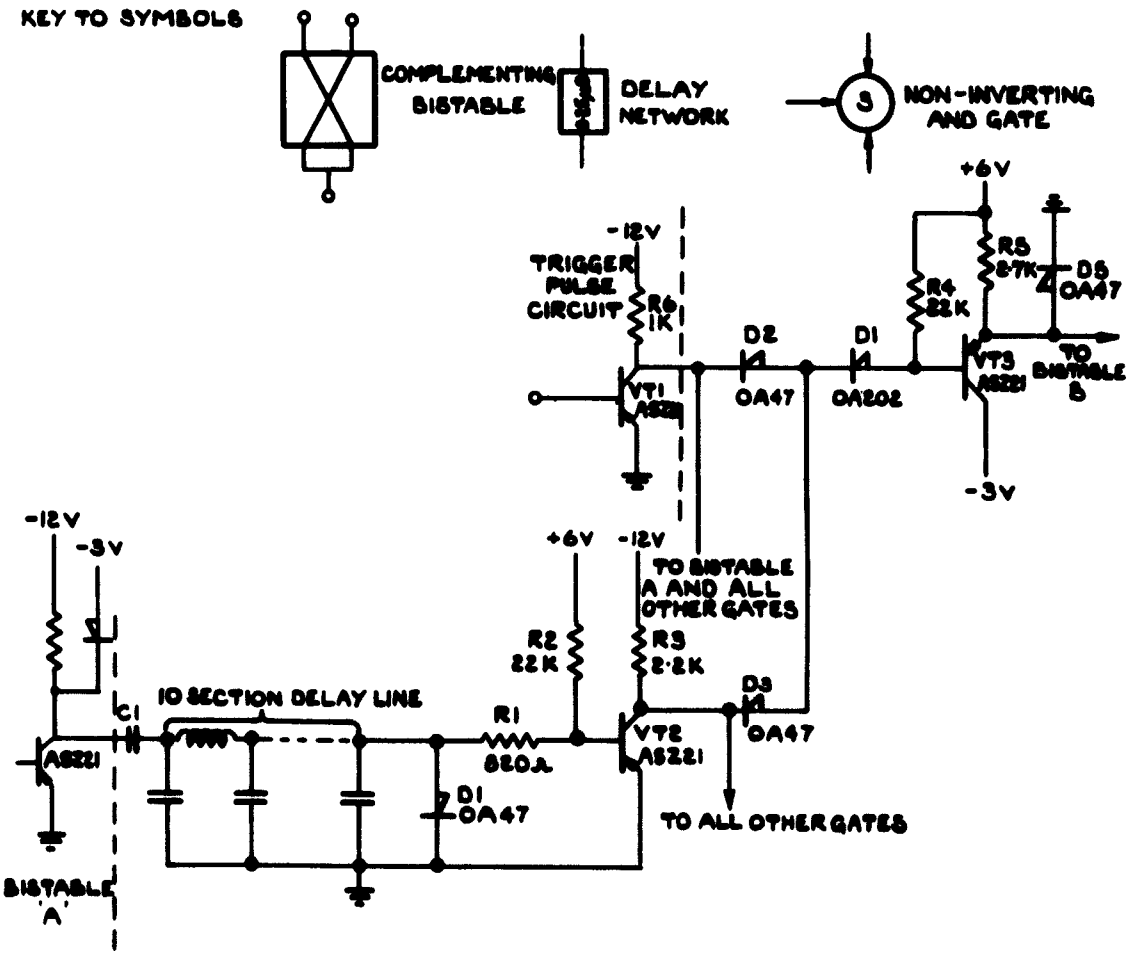


FIG.13(b) DELAY NETWORK AND GATE CIRCUIT.

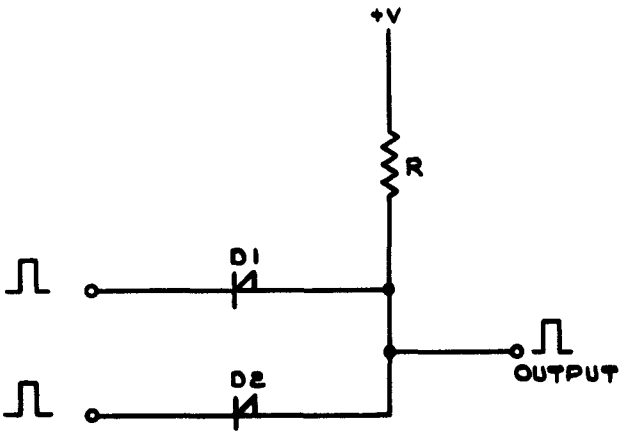


FIG 14(a) TWO INPUT RESISTANCE-RECTIFIER AND GATE

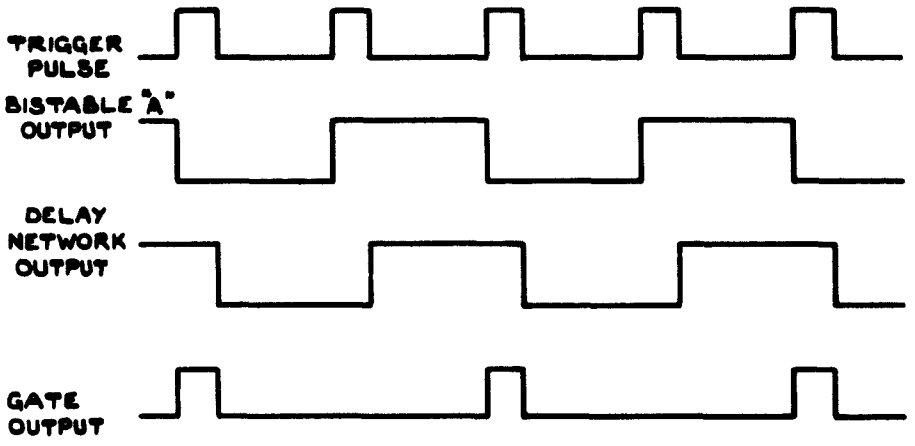


FIG. 14 (b) DELAY AND GATE CIRCUIT WAVEFORMS.

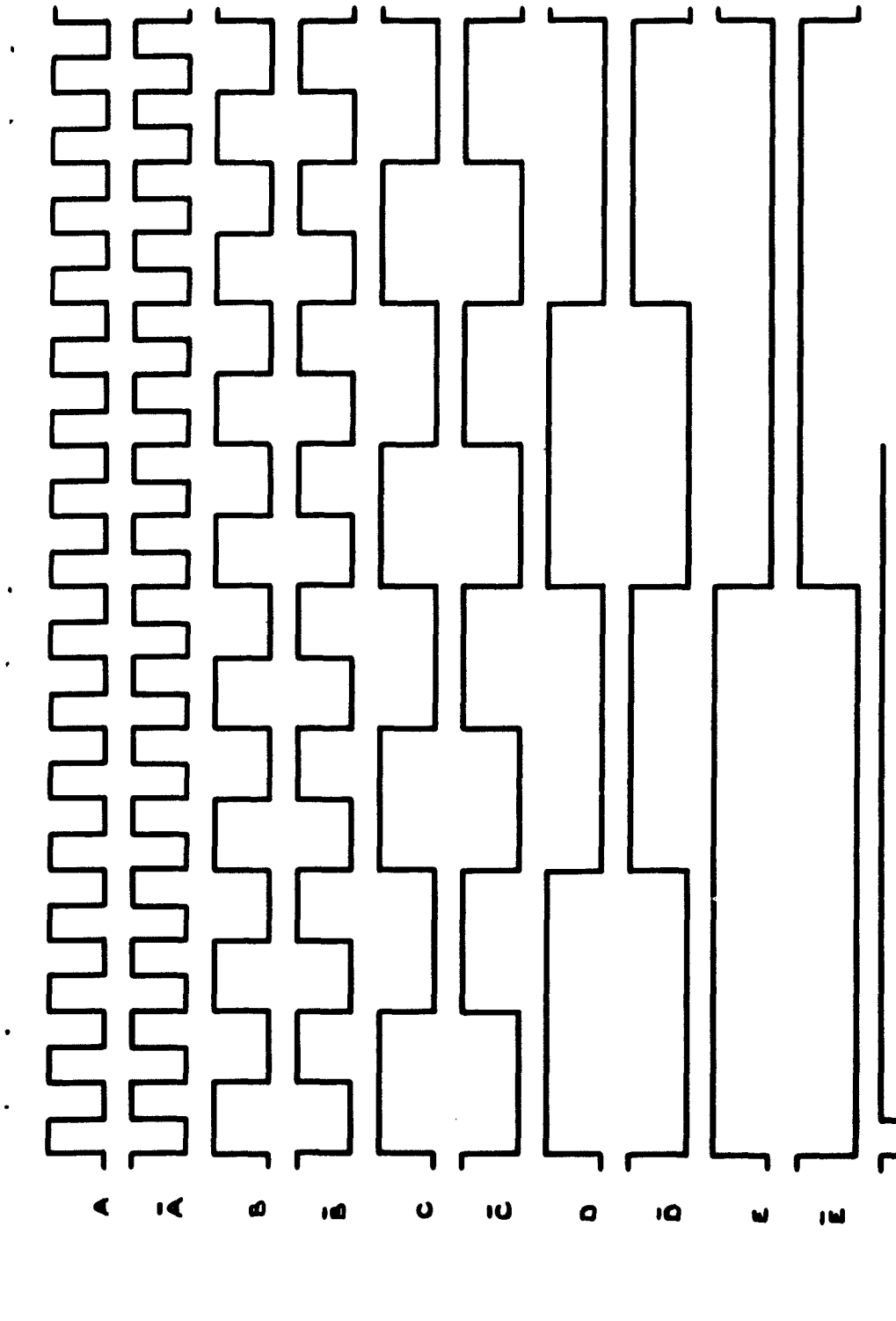


FIG. 15. FIVE DIGIT BINARY COUNTER WAVEFORMS.

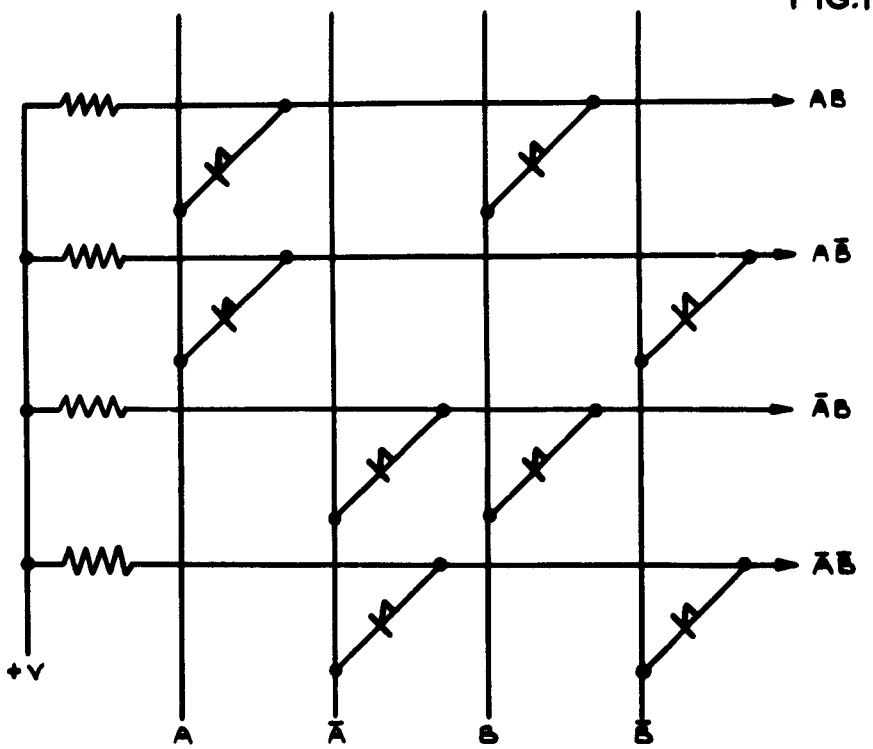


FIG. 16 (a) DIODE MATRIX FOR TWO VARIABLES.

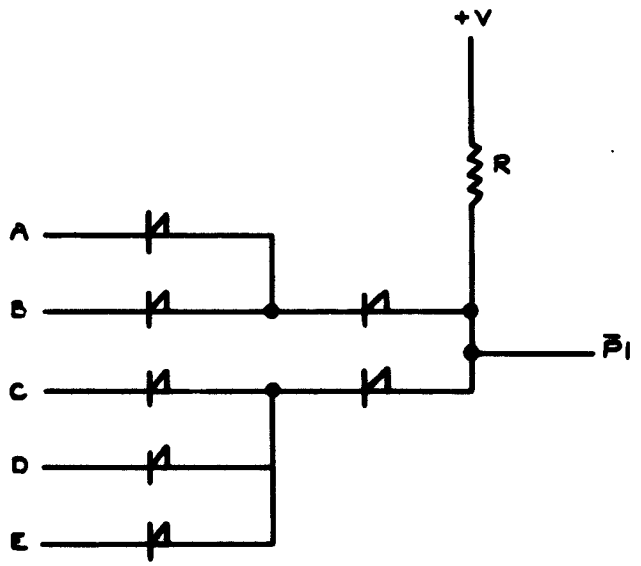


FIG. 16. (b) SELECTION CIRCUIT FOR P1.

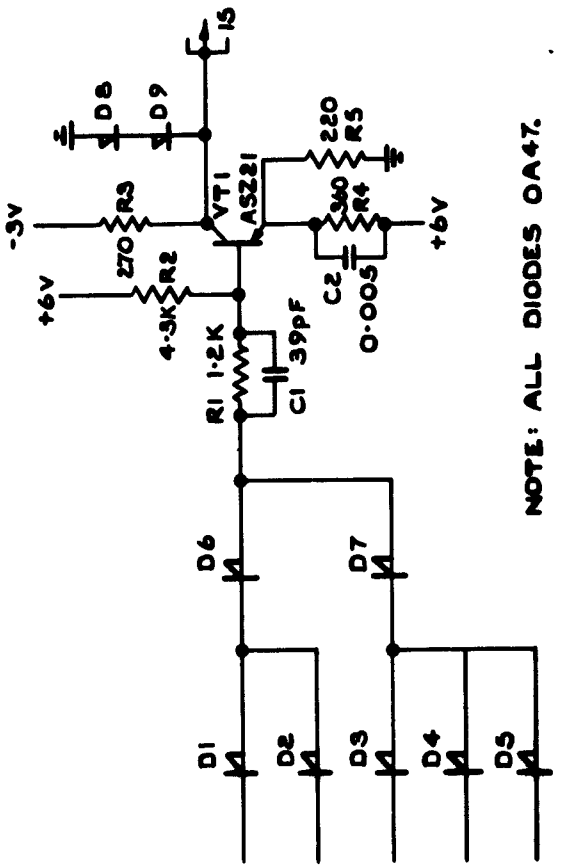


FIG.17. OUTPUT AMPLIFIER CIRCUIT DIAGRAM.

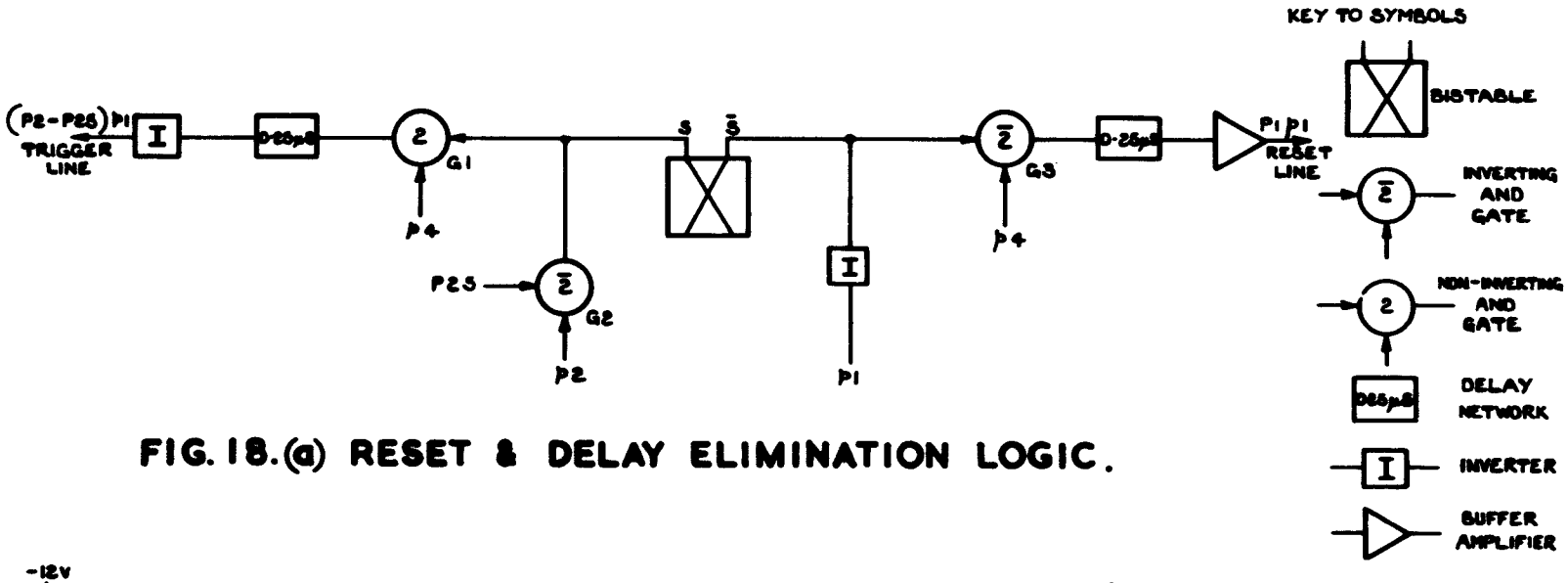


FIG. 18.(a) RESET & DELAY ELIMINATION LOGIC.

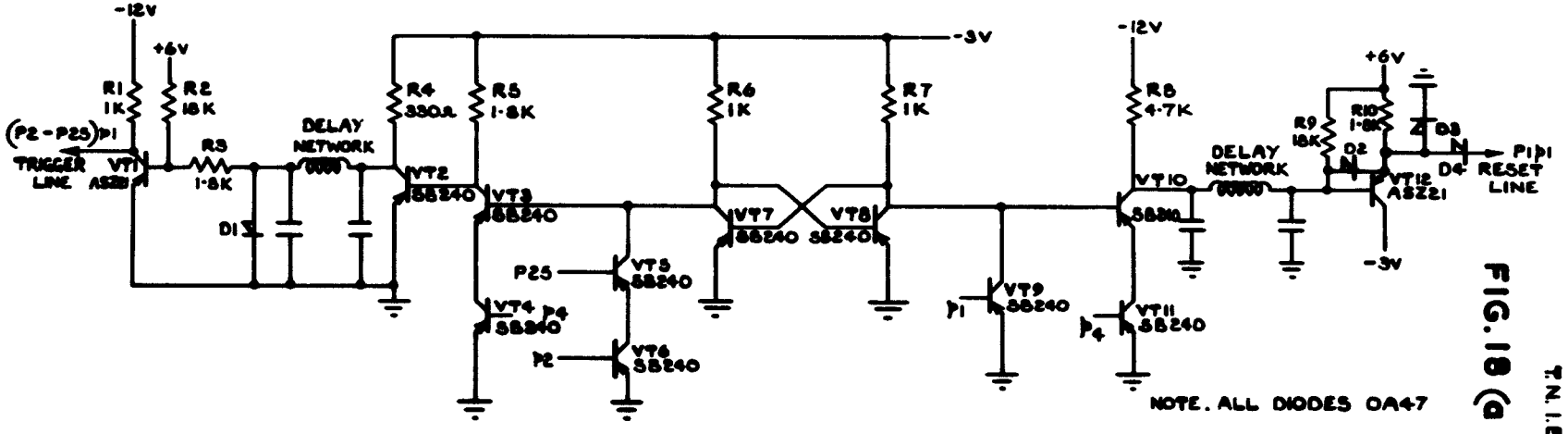


FIG. 18.(b) CIRCUIT DIAGRAM OF RESET & DELAY ELIMINATION NETWORK.

T.N. 1.E.E.3.

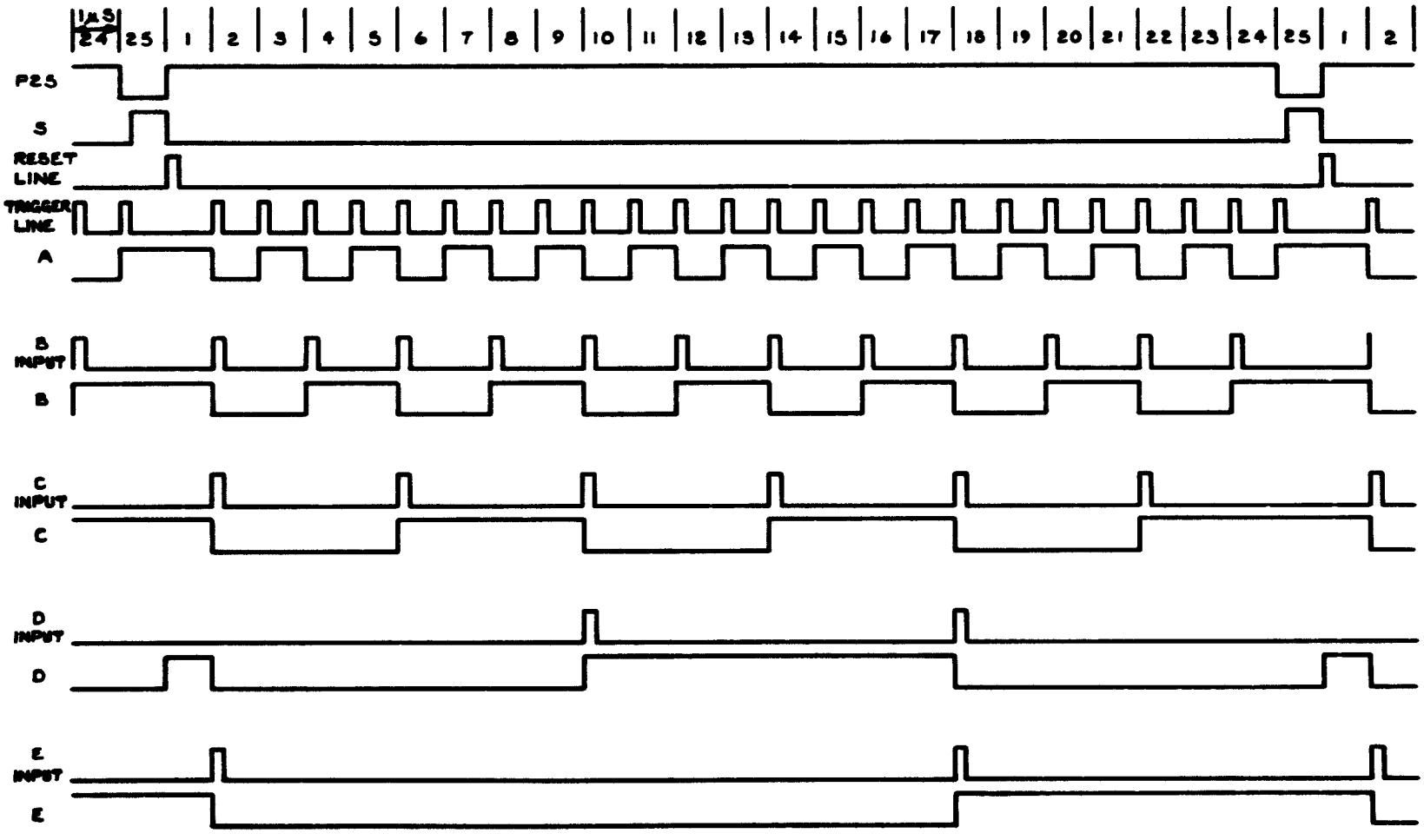
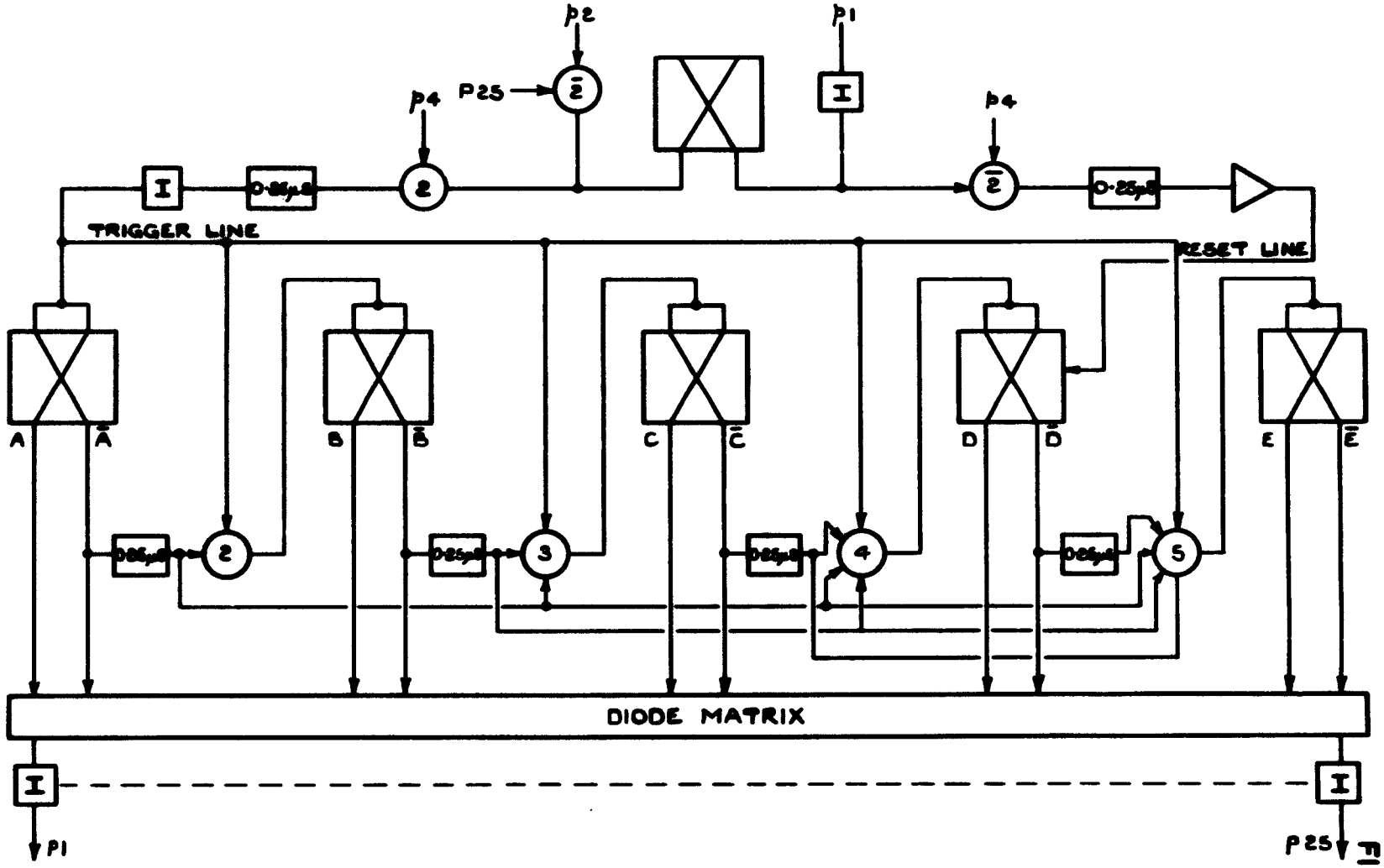


FIG. 19. WAVEFORMS OF P PULSE GENERATOR.

FIG. 19.



T.N. I.E.E. 33.

FIG. 20

FIG. 20. COMPLETE LOGIC DIAGRAM OF P PULSE GENERATOR.

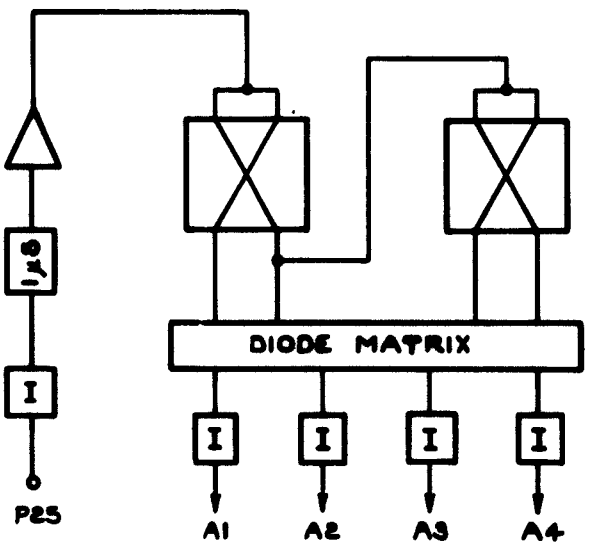


FIG. 21. LOGIC DIAGRAM OF A PULSE GENERATOR.

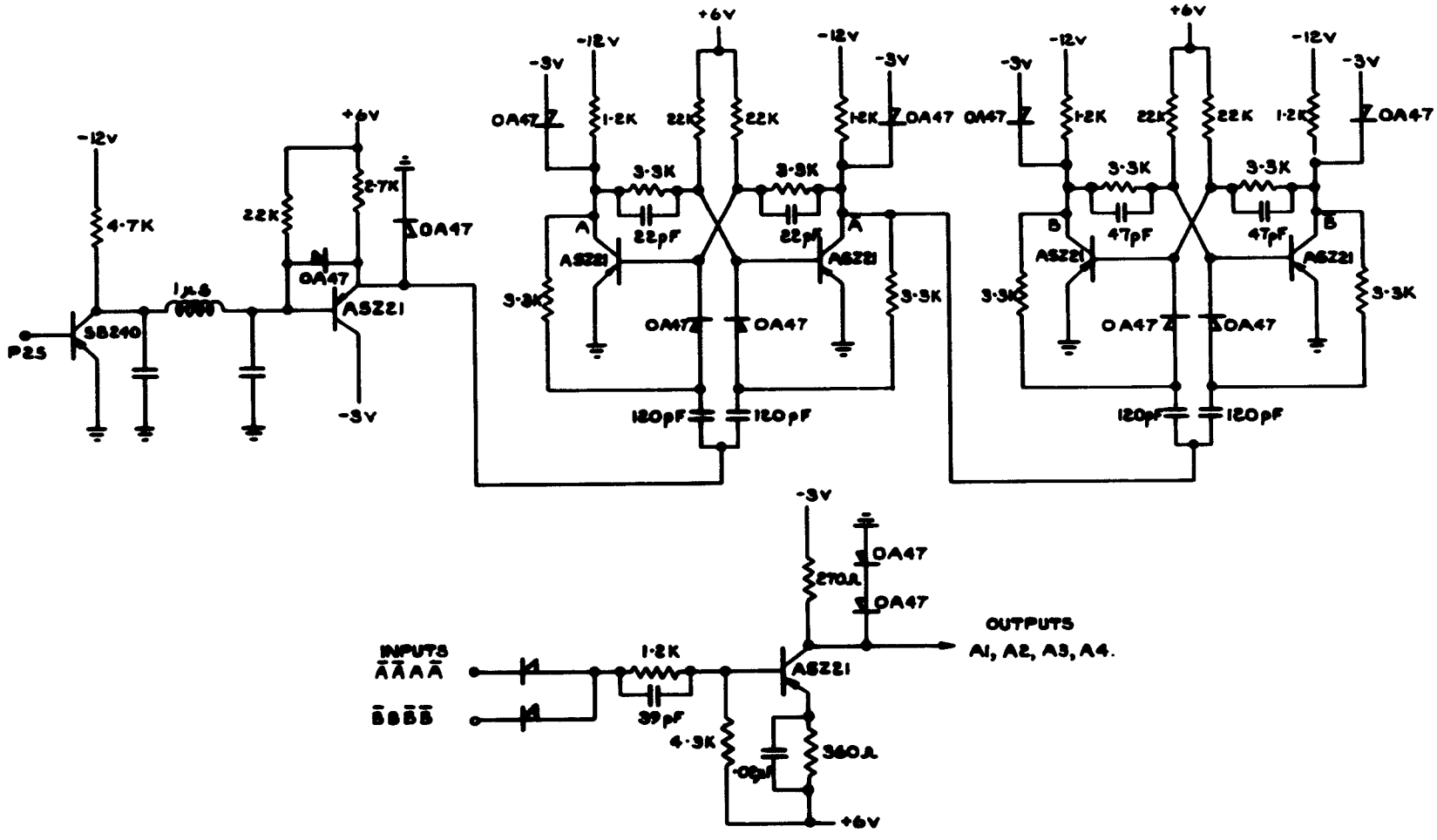


FIG.22. CIRCUIT DIAGRAM OF A PULSE GENERATOR.

T.N./E.E.33
FIG.22.

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TIMING PULSE GENERATION FOR A SYNCHRONOUS LOGIC SYSTEM.
Harris, R. December 1963.

A description is given of three pulse generators which produce related waveforms used in the control of a directly coupled logic system. The directly coupled transistor logic (DCTL) technique is first expounded in so far as it is relevent to the material in the text.

Each generator is considered first in general terms complete with the associated logic diagrams, and then a detailed description is given of the practical interpretation illustrated with schematic diagrams and waveforms.

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